Semiconductor Physics, Quantum Electronics & Optoelectronics, 2016. V. 19, N 1. P. 116-123.
doi: 10.15407/spqeo19.01.116

PACS 73.50.Gr, 84.32.Tt, 85.30.Tv

The charge trapping/emission processes in silicon nanocrystalline nonvolatile memory assisted by electric field and elevated temperatures

V.A. Ievtukh, V.V. Ulyanov, A.N. Nazarov
V. Lashkaryov Institute of Semiconductor Physics, NAS of Ukraine,
41, prospect Nauky, 03028 Kyiv, Ukraine
E-mail: v.ievtukh@gmail.com

Abstract. In this work, the influence of elevated temperatures on charge trapping in Si nanoclusters located in oxide layer of MOS structure has been comprehensively studied. The samples with one layer of nanocrystals in the oxide have been studied using the modular data acquisition setup for capacitance-voltage measurements. The memory window formation and memory window retention experimental methods were used with the aim to study the trapping/emission processes inside the dielectric layer of MOS capacitor memory within the defined range of elevated temperatures. The trap activation energy and charge localization were determined from measured temperature dependences of charge retention. The electric field dependence of the activation energy with subsequent charge emission law have been determined.

Keywords: nanocrystalline memory, MOS capacitor, charge trapping, elevated temperatures.

Manuscript received 25.11.15; revised version received 09.02.16; accepted for publication 16.03.16; published online 08.04.16.

1. Introduction

The most common parameters that characterizes memory as nonvolatile are the memory window and the data lifetime. The window width is defined by combination of write/erase voltage pulses applied to the gate during programming. The external electric field induced by programming pulses provokes the charge carrier trapping/emission processes in the oxide layer with formed nanocrystals as charge storage media. Once memory cell is programmed, the data retention stage begin. The data retention in nanocrystalline (NC) memory is commonly defined by intensity of charge emission processes from the NC layer of MOS oxide. The intensity of charge trapping/emission processes in the oxide, in turn, is mainly affected by presence of elevated temperatures and external electric fields. Varying these two parameters during the experiment allows one to study the physical processes related to nanocrystal memory operation and characteristics of the device, for instance, the charge activation energy (energy location of the traps determining the memory). The measurement setup and diagnostic methods specific for NCMs were developed for this aim [1]. In the present study, the devices based on MOS capacitor structure with floating gate made by one layer of silicon nanocrystals were considered. The methods and obtained experimental results for determination of memory

window width and charge retention were analyzed. The temperature and external electric field dependences of charge retention were measured with further determination of the trap activation energy, charge traps localization, the field dependence of charge emission.

2. Experimental samples and measurement setup

The samples based on metal-oxide-semiconductor (MOS) capacitor structure were used for the study. Samples were prepared on *p*-type silicon wafer with grown high quality thermal oxide of the thickness 3.5 nm. Next, amorphous silicon was deposited by LPCVD to the thickness 10 nm with subsequent recrystallization during thermal oxidation of amorphous layer. The samples were produced with one two-dimensional (2D) layer of self-aligned insulated Si nanocrystals in SiO_2 (Fig. 1a). The fabrication technology was described in more details in [2].

The capacitance-voltage (CV) measurement procedure was implemented to characterize MOS capacitor NCM samples. The hardware is presented in Fig. 1b and consists of: 1) sample holder equipped by heater and thermocouple for feedback; 2) proprietary high-speed high-frequency capacitance-voltage converter; 3) bias voltage amplifier; 4) temperature-control module with thermocouple signal converter for feedback; 5) National Instruments USB-6009 data acquisition system driven by 6) National Instruments LabView software.

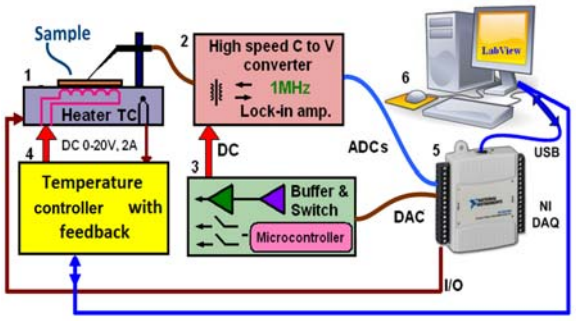
The high-speed (1 MHz) CV converter was specially designed to minimize the effect of measurements on the charge state of the object that opens the opportunity to study fast transient processes and provides sufficient precision of capacitance measurements. Setup allows one to heat and thermo-stabilize the sample up to temperature of 400 °C. The National Instruments USB-6009 module acts as the interface between software and hardware and consists of an analog-to-digital, digital-to-analog converters and digital input/output unit. The equipment allows to apply the programming pulses with different amplitude, polarity, duration to the sample, to change sample temperature and gate holding bias. The high frequency CV measurement method allows to receive several parameters of the sample and in particular flat band capacitance C_{fb} and voltage V_{fb} [3]. The V_{fb} shift after programming is proportional to amount of charge trapped in the dielectric.

The typical shift of CV caused by programming operation is shown in bold in Fig. 2. The left one is associated with the initial state ("erase") of the memory sample and the right one describes the memory sample in the charged state ("write").

The flat band voltage shift of the CV curve measured after the "Write" and "Erase" programming pulses is defined as *memory window*. This characteristic shows the difference of accumulated oxide charge between the "written" and "erased" memory states.

Al	*Gate contact*
SiO_2 3.5 nm	*Control oxide*
Si-nc 3 nm	*NC layer*
SiO_2 3.5 nm	*Tunnel oxide*
p-type Si	*Substrate*
Al	*Bottom contact*

a)



b)

Fig. 1. a) Silicon nanocrystal memory gate stack structures of single layered NC memory sample; b) measurement setup block schematic. 1) Sample holder, 2) C to V converter, 3) voltage amplifier module, 4) temperature controller, 5) data acquisition module NI USB-6009, 6) PC with NI LabView software.

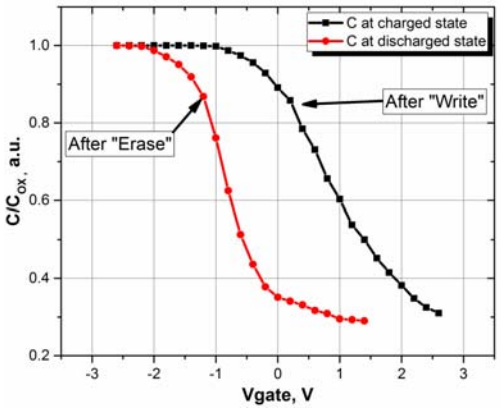


Fig. 2. Normalized capacitance-voltage characteristics (1 MHz) measured at charged (right) and initial (left) states.

3. Experimental methods

The experimental methods used for this study are based on alternate application of the programming bias pulse to the gate of the MOS structure pulse and measurement of the sample response. The elevated temperatures and holding gate bias are parameters of the experiment. In the study, the programming pulse of positive polarity corresponds to "Write" operation, and the programming pulse of negative polarity corresponds to "Erase" operation. In this way, "Write"/"Erase" operations are associated with negative charge trapping/detrapping in the floating gate of MOS structure.

Initial data values for each of the methods are determined from CV characteristic measured in direction from inversion to accumulation and backward at the beginning of the experiment. The flat-band voltage V_{fb} of

the memory structure gives information about the sign and magnitude of the charge stored in the floating gate. For this study, the memory *window formation* and *charge retention* experimental methods were used in combination with sample heating and gate biasing.

3.1. Memory window formation

The width of memory window is defined as difference of measured flat-band voltage values at "written" and "erased" states of the memory sample. This characteristic demonstrates an ability to store a charge in the floating gate of memory device. The value of memory window is given by the equation (1)

$$\Delta V_{fb} = \text{WINDOW} = V_{fb}^{"write"} - V_{fb}^{"erase"}, \qquad (1)$$

where $V_{fb}^{"write"}$ and $V_{fb}^{"erase"}$ are flat-band voltages of the memory cell determined after "write" and "erase" programming operations, correspondingly.

The developed method allows one to determine the programming mode with a maximal achievable memory window. The standard symmetrical programming sequence of successive "write" and "erase" pulses is shown in Fig. 3a and correspondent measured V_{fb} values evolution is shown in Fig. 3b.

The charge trapping and charge emission processes have different capture cross sections. So, in general, the maximal window value is unachievable at symmetric biasing as shown in Fig. 3a. The asymmetric biasing schemes (Figs 3c, 3d) are more desirable, as they allows to achieve an efficient trapping and emission in the course of re-programming. The programming sequence consists of program-erase pulse pairs with monotonically changed amplitudes. After application of each pulse of the series, the C-V dependence is measured with subsequent flat-band voltage (V_{fb}) determination. As a result, the memory window versus V_{pulse} curve is plotted.

3.2. Charge retention

Retention of accumulated charge is mainly defined by charge dissipation processes that take place in the nanostructured dielectric layer of the MOS structure. For a small size of nanoclusters, the physical nature of charge dissipation is predicted by the specific ratio of bulk-to-boundary silicon atoms in the nanocrystalline floating gate [4].

The leakage of charge could be measured using the mentioned above setup by application of programming ("write" or "erase") pulses with subsequent V_{fb} determination for different (in general) time periods (Fig. 4) [5].

Application of two parameters is possible for the charge retention experiment. The first one is elevation of the sample temperature, and the second one is variation of the gate bias applied to the sample during the retention process. The analysis of charge retention characteristics measured within the temperature domain allows one to determine the activation energy and localization of charge storage levels. Whereas the analysis of charge retention characteristics measured within the gate bias domain supplies information about charge emission process nature during retention measurements [6].

4. Experimental results and discussion

4.1. Memory window formation

For this study, the window formation method was used, and the memory window graph (Fig. 5) was plotted as the result. The result demonstrates the presence of a small amount of the initial positive charge in oxide. The latter fact can be explained by generation of positively charged defects in silicon dioxide layer at the production stage [7].

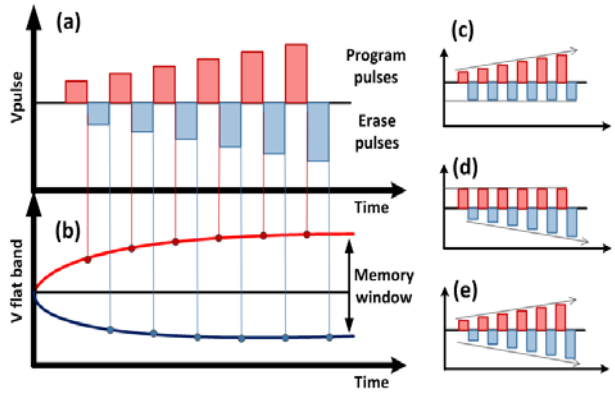


Fig. 3. Memory window formation algorithm. Series of programming pulses (a, c, d, e) with sequential V_{fb} determination after each pulse application (b).

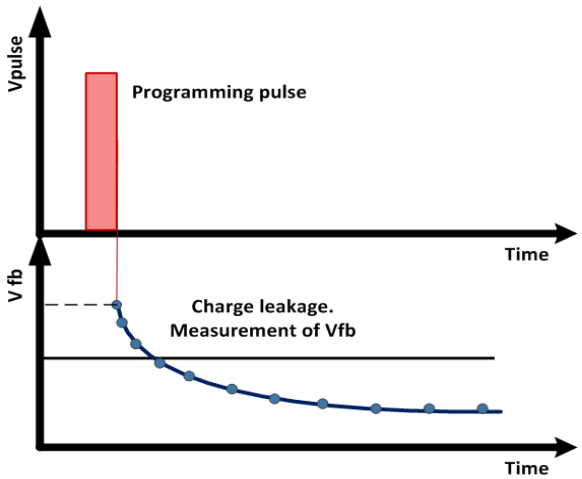


Fig. 4. Charge retention study diagram. The V_{fb} determination period could be varied to increase precision in fast parts of charge leakage process.

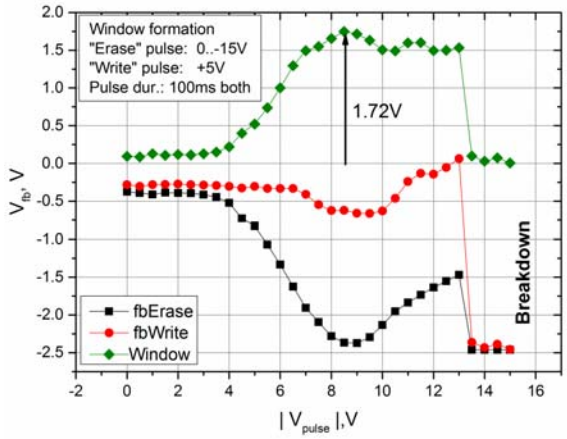


Fig. 5. Window formation results for single NC layered memory samples for the bipolar programming mode.

To study memory window formation in the bipolar programming mode, the series of "Write"-"Erase" pulse pairs were applied to the sample. The "Write" pulses have the constant amplitude of +5 V, whereas the "Erase" pulses have variable amplitude sweep from 0 to –15 V. The growth of the negative voltage amplitude of "Erase" pulse within the range from –4 V to –9 V is accompanied with the increase of positive charge in oxide. At the same time, application of the "Write" pulse with the constant amplitude +5 V restores oxide charge balance to initial state until "Erase" pulse amplitude becomes close to –7 V. At higher electric fields, the positive charge remains stored even after application of the "Write" pulse. For amplitudes of "Erase" pulse lower than –9 V, the amount of positive charge is decreased inversely. The negative charge trapping that is represented by injection of electrons from the gate through the control oxide layer takes place. Captured in NCs electrons tunnel to the substrate simultaneously, since the field direction is the same. Accumulation of charge in this case could occur, due to the fact that the charge injection rate from the gate exceeds the charge emission rate from NCs to the substrate. As both control and tunnel dielectrics are thin enough to make quantum mechanical tunneling available, the tunneling probability is a key factor that defines the total charge flow rate for the dielectric [8]. It was assumed that control oxide has a higher tunneling probability, as it has lower quality than the tunnel one, and the trap assisted tunneling process becomes possible. At very high electric fields, a big amount of negative charge is accumulated in NCs, which leads to high local electric fields that result in break-down of the dielectric layer.

The best result in window formation was achieved by fixing the pulse amplitude associated with electron trapping and varying another one. Determination of optimal programming mode for the studied samples of +5 V (100 ms) for the "write" pulse and –9 V (100 ms) for "erase" pulse, correspondingly, allowed one to measure the maximal memory window width of about 1.72 V. When the "erase" pulse amplitude is close to –4 V, the window increase is caused by increasing the trapped positive charge. The role of electron trapping is to compensate the previously accumulated positive charge. For the "write" voltage pulse of +5 V, the field in oxide close to 5 MV/cm is enough to emit electrons from substrate and compensate all the positive charge in nanoclusters or their vicinity. When the "erase" pulse amplitude is higher than –13 V, breakdown of dielectric occurs in the sample.

4.2. Temperature dependence of charge retention

To investigate the influence of elevated temperatures in the sample on physical processes responsible for the charge retention in nanocrystalline memory, the following study was performed. The optimal programming mode was taken from the memory window formation experiments and used for charge accumulation procedure in this study.

The charge retention measurement at elevated temperatures was separated by two parts.

- The window retention measurement where escape of both accumulated negative and positive charges was studied within the temperature domain.
- The negative charge retention measurement performed within both temperature and gate bias domains.

The setup presented in Fig. 1b can be configured to perform charge retention measurements in the window mode. The window retention measurements are important for nonvolatile memory characterization as they allows one to explore the time-evolution of the window width. Fig. 6 shows the window retention graph measured in the bipolar programming mode at elevated temperatures of the sample (25…150 °C) as the parameter. The window evolution graph with elevated temperatures as a parameter was determined from the data in Fig. 6 using Eq. (1) and presented in Fig. 7a in logarithmic time scale.

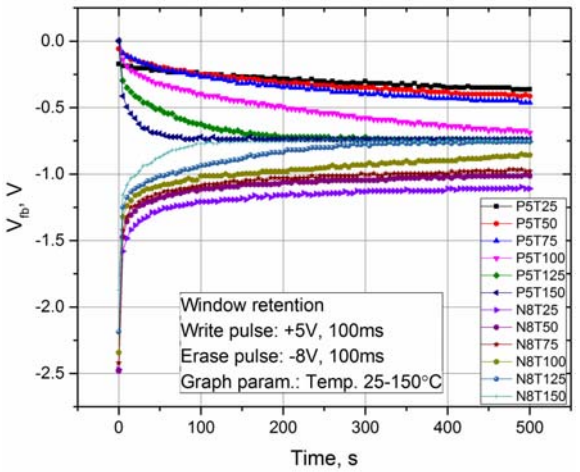


Fig. 6. Charge retention results for single NC layered memory samples for the bipolar programming mode. The families of negative charge retention and positive charge retention are presented.

It could be seen that the curves presented in Fig. 7a have linear regions at different sample temperatures. Hence, that regions could be fitted with exponential decay to find out window retention time constant versus the sample temperature. To derive the time constant of charge retention process from the retention curves, the fitting with ExpDec function (2) was used. The sample bias at retention measurements was zero.

$$Y = Y_0 + \sum_i A_i \cdot e^{\frac{-X}{t_i}}, \qquad (2)$$

where Y_0, A_i, t_i are the constants, determined by fitting procedure. As a result, the time constants graph of window retention are presented in Fig. 7b for different sample temperatures. It could be seen that window closeup speed is almost constant at sample temperatures up to 100 °C and noticeably increases at higher temperatures.

The time constant for each curve in Fig. 6 were determined using the plot of the retention time constant versus the sample temperature in Figs 8a and 8b, respectively, for negative and positive charge retention.

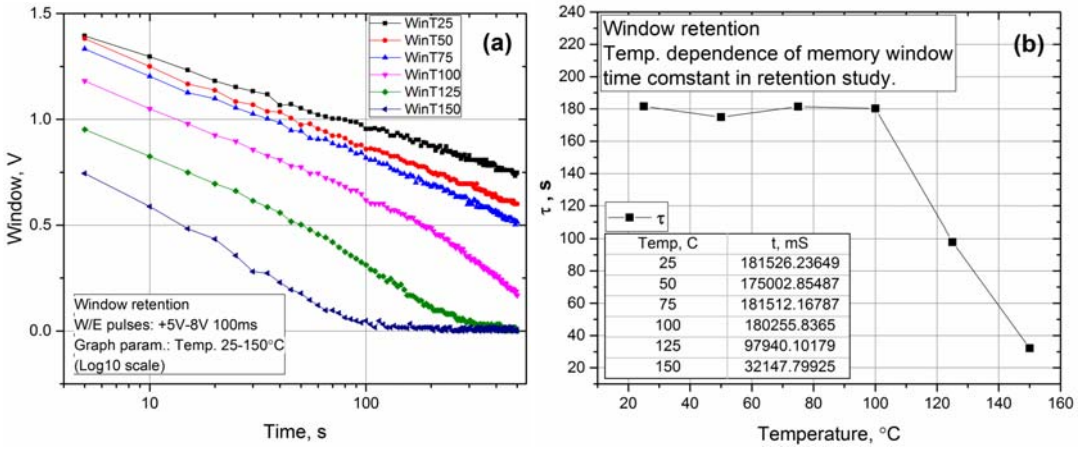


Fig. 7. a) Temperature dependence of window retention plotted in the Log10 time scale; b) temperature dependence of the time constant in retention study. Data points presented in inset.

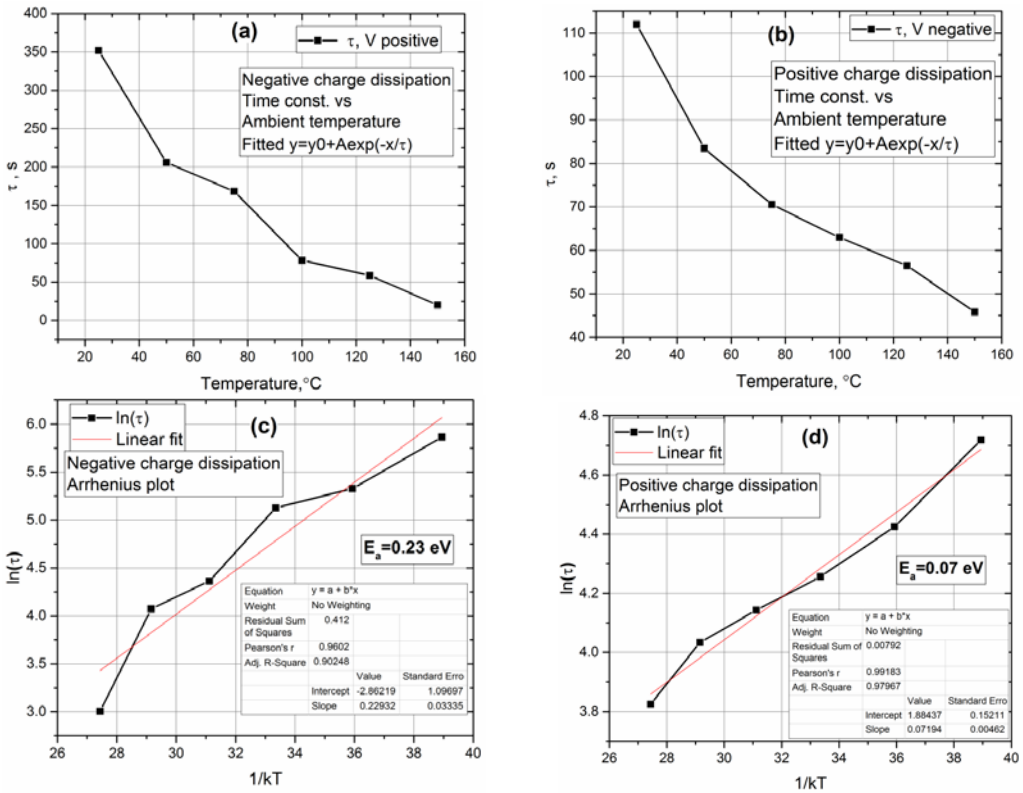


Fig. 8. Temperature dependence of time constants in charge retention measurement for accumulated negative (a) and positive (b) charges. The temperature dependence of time constants in charge retention measurement for accumulated negative (c) and positive (d) charges plotted in the Arrhenius coordinates with subsequent activation energy E_a determination.

The measured dependences were plotted in Arrhenius coordinates with subsequent linear fitting and activation energy E_a determination from the slope of the linear fit. Arrhenius plots of retention processes are presented in Figs 8c and 8d for negative and positive charge retention, respectively.

The negative charge retention dependences were fitted by exponential decay superposition. The single exponential decay fit of non-saturated curve parts gave satisfactory agreement with the experimental data. The time constant (τ) of each fitted plot was calculated with subsequent trap activation energy determination by plotting the temperature dependence of τ in Arrhenius coordinates:

$$\ln(\tau) = \Phi\left(\frac{1}{kT}\right) \qquad (3)$$

where k is the Boltzmann constant, T – temperature of the sample (for both samples). The *activation energy* E_a was found as the slope value of the linear fitted Arrhenius' plot (Fig. 8c). The plot has the single slope that corresponds to the activation energy 0.23±0.03 eV.

We consider electron transport as dominating in charge dissipation during retention process. The main dissipation mechanism is the charge emission from traps localized in nc-Si/SiO_2 interface to conduction band of substrate semiconductor.

The positive charge retention dependences were fitted by single exponential decay (Fig. 8b). The time constant (τ) of each fitted plot was calculated with subsequent trap activation energy determination by plotting the temperature dependence of τ in Arrhenius coordinates (Fig. 8d). The calculated activation energy value 0.07±0.012 eV is very small, which could be explained by participation of shallow traps in positive charge retention with quantum mechanical tunneling as main charge transport process.

4.3. Bias dependence of charge retention

With the aim to study charge emission law, the negative charge retention measurement was performed within both temperature and gate bias domains. The only part of results of accumulated negative charge retention measurement is presented for demonstration purposes. The charge retention results are presented in Fig. 9a for temperature (30…90 °C at the gate bias –0.6 V) domain and in Fig. 9b for gate bias (0…–1.2V at 50 °C) domain, respectively. For each gate bias value (0…–1.2 V) applied to the sample during retention, the temperature domain retention measurements were made. The retention time constant for each temperature value (25…150 °C) of the sample was determined, and the temperature dependence of time constant was plotted in Arrhenius coordinates with subsequent activation energy determination. As a result, the electric field dependence of activation energy was determined and presented in Fig. 10. Linearization of this dependence allows one to find out the charge emission law.

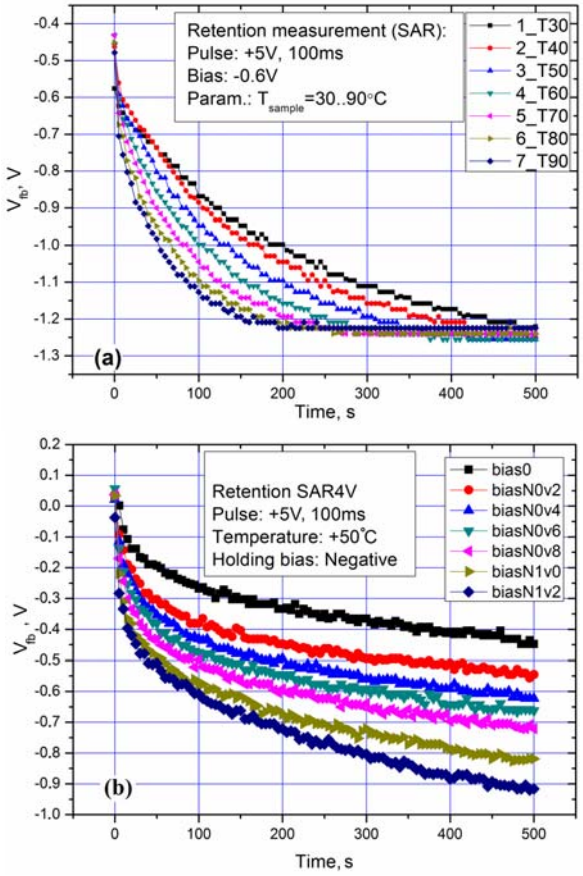


Fig. 9. Accumulated negative charge retention plots family for single NC layered samples after programming with temperature as parameter at fixed gate voltage (a) and gate voltage as parameter at fixed temperature (b).

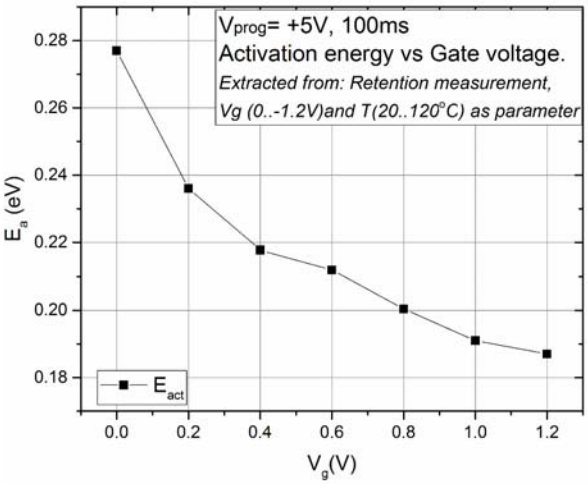


Fig. 10. Gate voltage (electric field) dependence of activation energy determined from negative charge dissipation measurements.

The typical emission mechanisms used to explain floating gate discharge in MOS nonvolatile memory devices are as follows: the Poole–Frenkel effect, direct tunneling, and Fowler–Nordheim tunneling [3]. The

barrier tunneling effects usually have a strong field dependence and weak temperature dependence. The authors assumed the Poole–Frenkel mechanism as responsible for device discharge, as the temperature dependence can be considered as noticeable. The Poole–Frenkel mechanism presumes lowering the trap potential barrier in the direction of the applied electrical field. In this state, electron requires less energy to escape from the trap.

In general, the field assisted emission of charge is defined by the activation energy and could be defined by the following expression:

$$E_a(\mathrm{E}_{ext}) = E_a^0 - \Delta\phi\,, \tag{4}$$

where E_{ext} is the external electric field, E_a^0 – trap activation energy at zero external electric field, $\Delta\phi$ – barrier decrease energy caused by the discharge law. The decrease in the activation energy that corresponds to the Poole–Frenkel mechanism is:

$$\Delta\phi_{\mathrm{PF}} = e\sqrt{\frac{e}{\pi\varepsilon_0\varepsilon_d}}\sqrt{\mathrm{E}_{ext}}\,, \tag{5}$$

where ε_d is the relative permittivity of the dielectric (SiO_2).

The dependence presented in Fig. 10 was successfully linearized by taking square root from the external electric field axis (Fig. 11). The latter was calculated using the applied gate voltage value and the sample dielectric thickness (see Fig. 1a). The latter confirms that Pool–Frenkel barrier lowering is responsible for negative charge emission during negative charge retention measurements. Lowering the Poole–Frenkel barrier is demonstrated by inset of Fig. 11. From the obtained experimental dependence of activation energy vs. electric field, we can extract energy location of the trap that emits charge during the charge retention process, and it is equal to 0.28±0.01 eV.

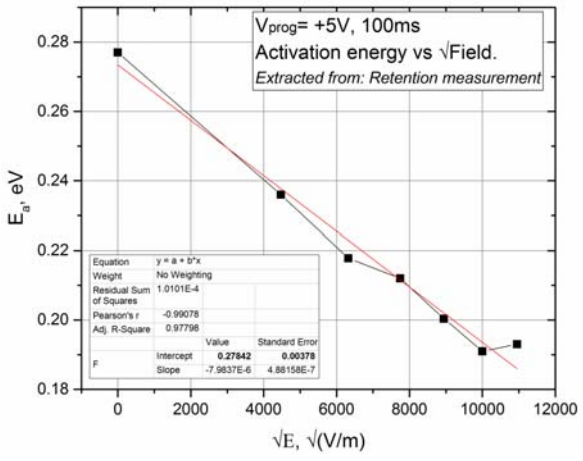


Fig. 11. Linearized electric field dependence of the activation energy of charge dissipation during the retention process. The Poole–Frenkel barrier lowering is demonstrated in the inset.

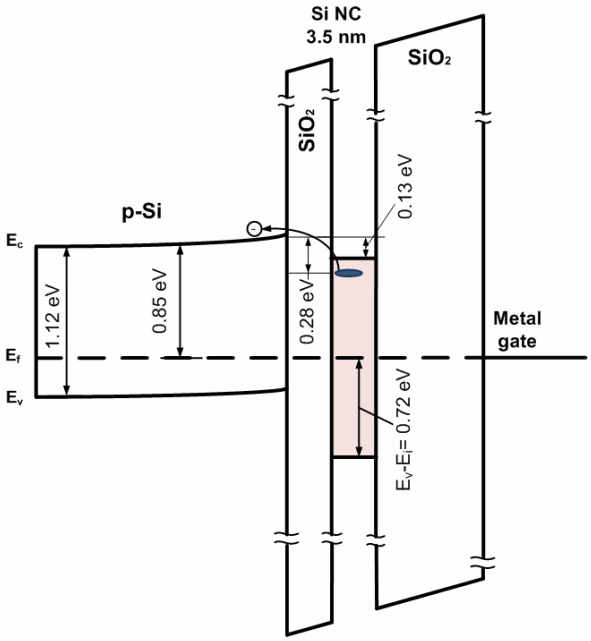


Fig. 12. Energy band diagram of the studied nanocrystaline memory device.

To estimate trap localization in the bandgap of our gate dielectric, the nanocrystal energy band diagram has to be built. The Fermi level of substrate semiconductor 0.85 eV was calculated for the concentration of acceptors 10^{15} cm^{-3} measured experimentally from the capacitance-voltage dependence of the sample. We have assumed that silicon nanocrystals have an intrinsic carrier density and a spherical shape. The nanocrystal bandgap widening calculations were performed to take into account the quantum confinement effect [9]. For nanocrystal sizes 3.0, 3.5, and 5.0 nm, the bandgap values are 1.553, 1.438, and 1.276 eV, correspondingly. The band diagram for single layered nanocrystal sample is presented in Fig. 12.

5. Conclusions

The charge retention measurements of nanocrystalline memory device have been performed within both elevated temperature and gate bias domains. The charge trap activation energy and charge localization have been determined using the measured temperature and bias dependences of charge retention. It has been shown that charge emission from memory traps is caused by thermal activation combined with the Pool–Frenkel mechanism.

References

1. V.A. Ievtukh, A.N. Nazarov, V.S. Lysenko, Nano-cluster NVM Cells Metrology: Window Formation, Relaxation and Charge Retention Measurements // *AMR*, **718-720**, p. 1118-1123 (2013).

2. A. Salonidou et al., Silicon nanocrystal memories by LPCVD of amorphous silicon, followed by solid phase crystallization and thermal oxidation // *Nanotech*. **15**, p. 1223 (2004).
3. S.M. Sze // *Physics of Semiconductor Devices*, 2-nd ed. John Wiley&Sons, NY, 1981.
4. V.-Y. Aaron, J.-P. Leburton, Flash memory: Towards single-electronics // *IEEE Potentials*, **21**, p. 35-41 (2002).
5. V.I. Turchanikov, V.S. Lysenko, A.N. Nazarov, V.A. Ievtukh, M.M. Lokshin, The way to determine the time constant for charge storage in dielectric cells of nanocrystalline energy-independent memory possessing the structure metal-dielectric-semconductor // *UA Patent* №108830 (10.06.2015).
6. V.I. Turchanikov, A.N. Nazarov, V.S. Lysenko et al., Charge trapping in Si-implanted SiO_2-Si memory devices at high electric fields and elevated temperatures // *J. Phys.: Conference Series*, **10**, p. 409-412 (2005).
7. V. Ievtukh, A. Nazarov, V. Turchanikov et al., Charge accumulation in the dielectric of the nanocluster NVM MOS structures under anti- and unipolar W/E window formation // *Microel. Rel*. **47**, p. 626-630 (2007).
8. V. Ievtukh, A. Nazarov, V. Turchanikov et al., Charge trapping processes at memory window formation in single- and double nanocrystal layered NVMs // *Microel. Eng*. **109**, p. 5-9 (2013).
9. C. Murphy et al., Quantum Dots: A Primer // *Appl. Specroscopy*, **56**/1, p. 16 (2002).