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INTEGRAL NONLINEARITY OF SECOND-ORDER SINGLE-BIT SIGMA-DELTA MODULATOR

Sun Haimeng[1], R. Kochan[2], O. Kochan[2], Su Jun[3]
[1] – Jimei University Chengyi College, 185 Yinjiang Road, 361021, XiaMen, China,
[2] – Lviv Polytechnic National University,
12 Bandera str., Lviv, 79013, Ukraine. E-mail: kochan.roman@gmail.com
[3] – Hubei University of Technology, Wuhan, 430068, China.

The simulation model of single-bit second-order sigma-delta modulator and analog-to-digital converter (ADC) based on this modulator is developed. The study of influence of all components parameters on integral nonlinearity of ADC is carried out by the model. As revealed, there are no influence of second integrator nonlinearity on ADC nonlinearity.
References 16, figures 9, table 1.
Key words: sigma-Delta Modulator, Integral Nonlinearity, Error Correction.

Introduction. Wide implementation of processors and digital signal processing algorithms in data acquisition and measurement systems brings to that analog-to-digital converters (ADC) became the necessary component of such systems. The metrology characteristics of systems of electrical quantities measurement are mainly defined by metrology characteristics of used ADCs. Therefore, improvement of metrology characteristics of ADCs is an actual task and it can give improvement of the accuracy of measurement results.

The segment of precision ADC is filled by the converters based on sigma-delta modulators (SDM). Such ADCs are in the line of leading companies and are very popular on the market [1, 2]. Their high accuracy is based on implementation of accuracy improvement methods – null setting and calibration using reference voltage source. These methods provide correction of additive and multiplicative components of ADC's error. The residual error of such ADC is mainly defined by nonlinearity of ADC's conversion function (CF). Its level is significant and potentially we can decrease it. For example, 24-bit ADC of AD7714 type has integral nonlinearity not more than 15 ppm [3], and it corresponds only to 16-th bit. At the same time its effective resolution is up to 22 bit. So the nonlinearity of CF is 6 low signed "effective" bits or 8 least significant bits - LSB (taking into consideration noise level). Decreasing of ADC's nonlinearity provides smoothing of ADC's CF and can provide design accurate model of measured object [4, 5] or process [6, 7]. Therefore it is actual to investigate the form of ADC's nonlinearity.

The complexity of ADC's nonlinearity correction is associated with its dualistic character: nonlinearity is systematic for each ADC and random for the set of single type ADC. Besides the parameters of nonlinearity approximation function depend of the operation mode of ADC. Therefore, the single determination of this function, for example, after manufacturing, and further correction do not provide significant accuracy improvement of conversion results.

The set of methods is developed. They provide precision identification of ADC's CF in the set of testing points [8]. The number of generated testing points is beginning from one up to some dozen per range depending on the complexity of the circuit and processing algorithm. However the implementation of these methods for correction of nonlinear error of ADC demands forming of interpolation curve for whole range. The interpolation function selection demands investigation of its character. The nonlinearity of sigma-delta ADC's CF is defined by nonlinearity of forward signal channel [9, 10] and the purposeful selecting of interpolation function for nonlinearity correction demands study of the influence of integrator nonlinearity on nonlinearity of SDM and ADC based on SDM. So, **the objective of the presented work** is to investigate the character of ADC's CF nonlinearity for adequate forming of interpolation curve.

Development of simulation model. The exclusively experimental investigation of dependence of SDM's nonlinearity on integrators' nonlinearity could not be informative enough because of:

- influence of the error of reference equipment;
- complexity of precision owing to integrator nonlinearity.

Therefore it is proposed to make investigation by simulation. The results obtained in [10, 11] suppose the synchronous variation of the parameters of all integrators. This is only one and not typical case for high order SDM because each integrator is separate component with own parameters and essential divergence between their time constants [11]. Therefore it necessary to investigate the sensitivity of SDM's nonlinearity for the cases of independent integrators and their nonsynchronous combinations.

The structure of single-bit second-order SDM is presented in fig.1. It consists of forward signal and backward signal channels. The first of them consists of two adders – ⊗, two integrators – ∫ and synchronous comparator – SC (which consists of asynchronous comparator and synchronous D-triger – TT). Backward signal channel consists of single-bit

digital-to-analog converter – DAC, which is controlled by output code of SDM. Synchronization pulses for TT are generated by pulse generator – G.

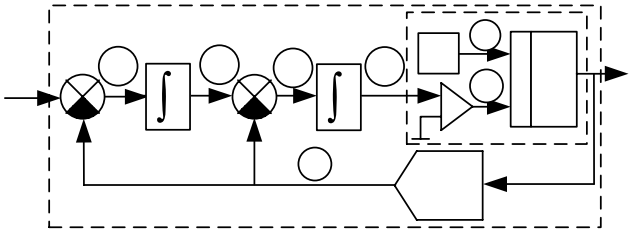


Fig. 1

The testing points of SDM (S1, S2, I1, I2, G, C, D) are marked in fig. 1. The dependences of voltage at these testing points on current are expressed by component equation of simulation model. The system of equations second-order SDM is

$$\begin{cases} U_{S1}(t) = U_X(t) - U_D(t), \\ U_{I1}(t) = \dfrac{1}{\tau_1}\int_0^t U_{S1}(t)\,dt, \\ U_{S2}(t) = U_{I1}(t) - U_D(t), \\ U_{I2}(t) = \dfrac{1}{\tau_2}\int_0^t U_{S1}(t)\,dt, \\ U_C(t) = \begin{cases} 1, U_{I2}(t) > 0 \\ 0, U_{I2}(t) \le 0 \end{cases}, \\ U_G(t) = \begin{cases} 1, t \in \left[k \times T, (k+0{,}5) \times T\right], \\ 0, t \in \left((k+0{,}5) \times T, (k+1) \times T\right), \end{cases} \\ N_X(t) = \begin{cases} U_C(t), \left(U_G(t) = 1\right) \wedge \left(U_G(t - \Delta t) = 0\right), \\ N_X(t - \Delta t), \end{cases} \\ U_D(t) = \begin{cases} E, N_X(t) = 1, \\ -E, N_X(t) = 0, \end{cases} \end{cases} \quad (1)$$

where U_X is the input voltage; N_X is the output pulse sequence, which corresponds to input voltage U_X; $U_{S1}, U_{S2}, U_{I1}, U_{I2}, U_C, U_G, U_D$ are the voltages of appropriate testing points of SDM; τ_1, τ_2 are the time constants of appropriate integrator; T is the period of pulse generator; k is the integer value; $\Delta t \to 0$ is the time step of simulation; E is the output voltage of DAC.

Taking into consideration (1) and the discreteness of output signal of SDM for the analog-to-digital conversion n is computed as

$$n = \sum_{i=l}^{l+M} N_X(i \times T). \quad (2)$$

where $M = 2^K$ is the maximum number of counts of ADC, which is defined by its resolution K; $t1$ is the time of integrator "entry" into operating mode (after transient process of periodic waveform shaping); $l = \dfrac{t1}{T}$ is the number of output signals during time $t1$, which are nonregistered because of nonfinishing of transient process.

The input voltage of ADC is computed by expression

$$U'_X = 2 \times E\left(\frac{n}{M} - 0{,}5\right). \quad (3)$$

The difference between input voltages defined by (1) and computed in (3) forms error, which is taken into consideration during analysis

$$\Delta = U_X - U'_X. \quad (4)$$

The main parameters, which cause the integrator nonlinearity, are the limited frequency band and limited gain of amplifier. The significant effect of these parameters is provided by rather high operating frequency of integrators, which corresponds to operating frequency of pulse generator. This frequency, for example, for ADC of AD7714 type, is 1 or 2,5 MHz. Some works [9, 11] show the negligible influence of amplifiers limited frequency band on SDM nonlinearity. Therefore it is rational, first of all, to investigate the influence of amplifiers limited gain on ADCs nonlinearity.

This influence we can simulate by linear variation of integrator's time constant in equation (1) depending on input signal. It gives the parabolic approximation of integrator CF after integration.

$$\tau_i = \tau_{0i} \times \left(1 + s \times k_{\tau i} \times U'_{Ii}\right); \qquad s = \begin{cases} -1, U'_{Ii} > 0 \\ +1, U'_{Ii} < 0 \end{cases}; \qquad i = \overline{1,2}, \tag{5}$$

where τ_{0i} is the "initial" value of time constant of i-th integrator; s is the multiplier, which provides symmetric variation of time constant for positive and negative input signals; $k_{\tau i}$ is the value for variation of time constant of i-th integrator; U'_{Ii} is the output signal of i-th integrator at previous simulation step.

The developed simulation model is oriented on analysis in time domain and realizes the approach of asynchronous incrementing modeling with constant time step.

U_{XMAX}	2,5	3	3,5	4	4,5
$1/\tau_1$	3.3×10^4	2.4×10^4	1.7×10^4	1.1×10^4	5.2×10^3
$1/\tau_2$	5×10^4				

According to [12] the range of SDM and ADC based on SDM is defined by output voltage of backward DAC, frequency of pulse generator and time constants of integrators. The parameters of several SDMs are computed. These parameters are presented in table. The variants of ADCs are given in the line with U_{XMAX}. All SDMs in this table provide frequency of pulse generator of 100 kHz, DAC voltage is ± 5 V.

Verification of simulation model. The verification of the developed simulation model is implemented by analysis of the ADC parameter based on linear model of SDM (1) and model of SDM with taking into account the integrator nonlinearity. The CF of ADC based on linear model of SDM is step function, approximated by segments of the line, which covers the origin of coordinates. The approximation error does not exceed the sensitivity of ADC. The integral nonlinearity of this model is equal to zero over all the range. The oscillograms of signals at all testing points for all SDMs from table for input voltages of 0 and U_{XMAX} correspond to appropriate signals given in [13-15]. Some of these oscillograms is presented in fig. 2. The maximum value of all integrator output signal does not exceed voltage of DAC. It means that SDM operates correctly and in linear mode. Therefore we can consider adequate linear simulation model of SDM with parameters from table.

The influence of integrator nonlinearity on output signal is described by (5). It gives distortion of all SDM's signals in comparison with linear model. Therefore it is impossible to see the influence of nonlinearity by subtraction the signals in appropriate time. The example of SDM's signals with nonlinear integrators is presented in fig. 3. These signals are for the identical conditions and time to the signals presented in fig. 2. As seen, these signals are significant different.

The nonlinearity of the first integrator can be seen by plotting imagining straight line through two extremums at the ends of segments of polyline, which indicates this integrator output signal.

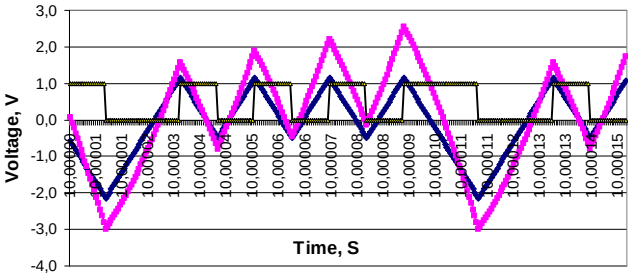
The plot of the first integrator nonlinearity is presented in fig 4. This line is the segment of parabola and it corresponds to data in [16]. Therefore the simulation of integrator nonlinearity, at least for the first integrator, is adequate and correct.

The analogical detection of the second integrator nonlinearity is impossible because of nonlinear character of output signal with unknown parameters even for linear model of SDM. Therefore, the influence of integrator nonlinearity on statistical parameters of SDM output signal is analyzed as following. SDM output signals with all linear integrators and one nonlinear integrator are compared. The distortion level of SDM with nonlinear first integrator for SDMs from table depending on input voltage is presented in fig. 5. The nonlinearity of the first integrator is equal to 0,1 %. Generally the nonlinearity of 0,1 % of the first integrator gives 5…50 % distortion of SDM output signal.

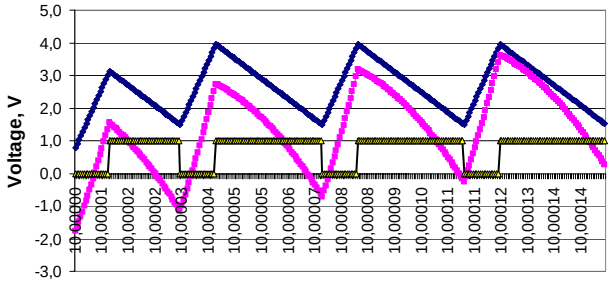
The distortion level of SDM with nonlinear second integrator for the same SDMs is presented in fig. 6. In this case, all curves are random but total distortion level is less than in the case of nonlinear first integrator. Generally the nonlinearity 0,1 % of the second integrator gives 1,6…45 % distortion of SDM output signal.

The distortion level caused by nonlinearity of the second integrator is 1,1 … 3 times less than distortion level caused by nonlinearity of the first one. We explain this by longer way of distorted signal of the first integrator in comparison with the second one. The trend of all curves presented in fig. 6 is declined. We explain this by decreasing the frequency of integrator output signals in the case of increasing input voltage. It gives the longer sequence of stable comparator output signal and decreasing of total number of comparator switchings. Therefore the delay of comparator output signal has less influence on conversion result. The random character of curves we can explain by close loop of SDM structure and the great step of input voltage simulation. The presented results of developed simulation model confirm its simplicity, adequacy and informativity. Therefore, we can use this model to study the properties of second-order SDM.

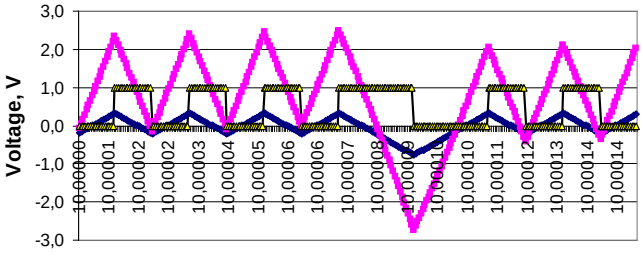
Investigation of Integrator Nonlinearity influence on SDM Nonlinearity. The analysis of integrator nonlinearity influence and integral nonlinearity of ADC based on SDM is realized by computation of the absolute error of conversion results using (4). The investigation is carried out for all SDMs presented in table. The level of simulated integrator nonlinearity is 0,01…10 %. The dependence of ADC integral nonlinearity for different SDMs is presented in fig 7. These curves are obtained for first integrator nonlinearity of 0,1 %. The proportional curves are obtained for other levels of this integrator nonlinearity. The dependence of maximum nonlinearity of SDM on first integrator nonlinearity levels is presented in fig. 8.



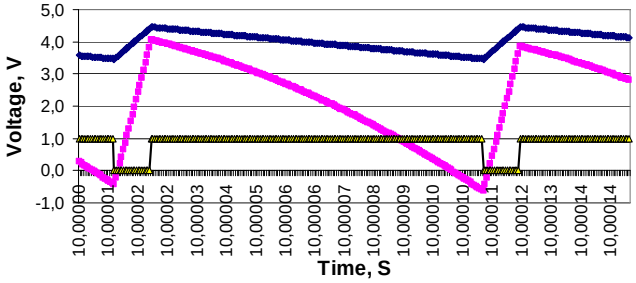
$U_X = 0$ В; $U_{XMAX} = 2{,}5$ В



$U_X = U_{XMAX} = 2{,}5$ В



$U_X = 0$ В; $U_{XMAX} = 4$ В



$U_X = U_{XMAX} = 4$ В

Fig. 2

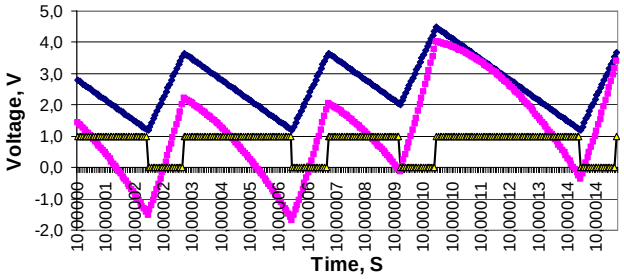


Fig. 3 $U_X = 2{,}5$ В; $U_{XMAX} = 2{,}5$ В

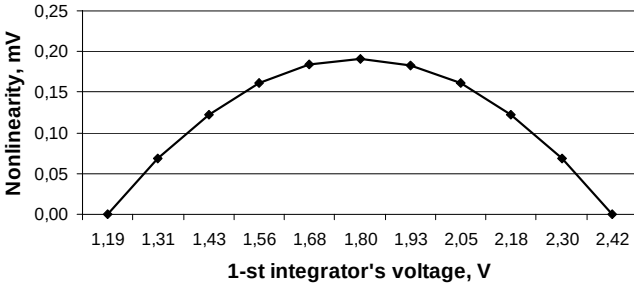


Fig. 4

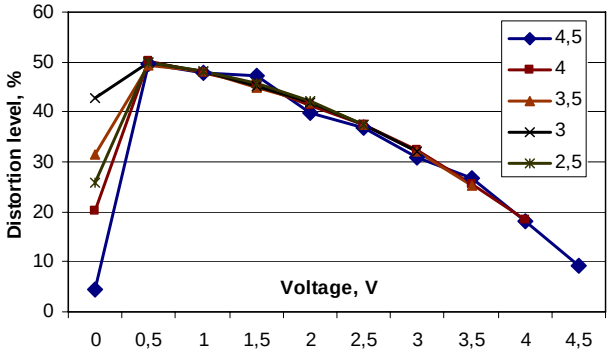


Fig. 5

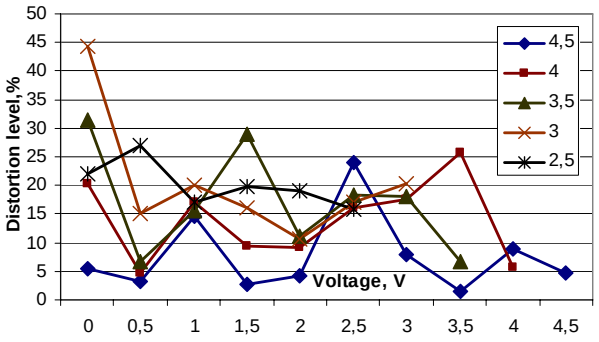


Fig. 6

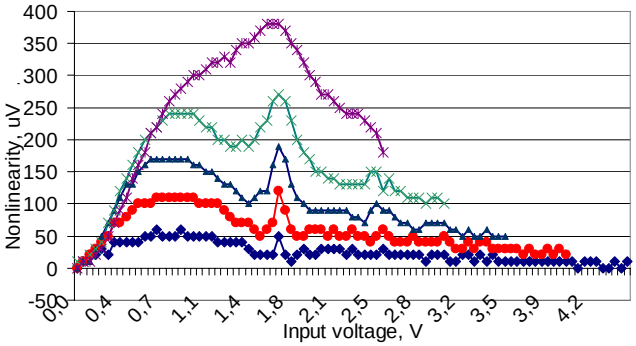


Fig. 7

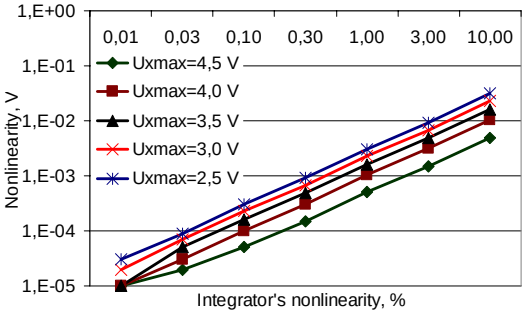


Fig. 8

Taking into consideration curves presented in fig. 8 we can compute the nonlinearity rejection factor using the expression $$K = \frac{\Delta_{UI1}\delta_{NL}}{\Delta_{NL}100\%},$$

where Δ_{UI1} is the peak-to-peak of first integrator output signal, δ_{NL} is the relative nonlinearity of integrator, Δ_{NL} is the nonlinearity of SDM.

The plots of nonlinearity rejection factor for nonlinear first integrator are presented in fig. 9. As shown, this factor is approximately constant for nonlinearity more than 0,03 %. The value of the rejection factor is equal to 8…10 and SDMs with less range provide less values of rejection factor. The nonlinearity level less than 0,03 % corresponds to removable value of rejection factor. It could be explained by resolution of SDM model.

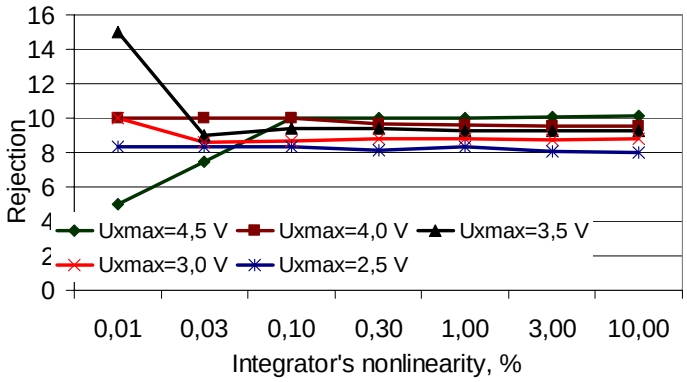


Fig. 9

The methodology of investigation of the second integrator nonlinearity influence on SDM nonlinearity is identical to the first integrator. Generally five SDMs presented in table I with seven nonlinearity levels from 0,01 to 10 % are studed. The input voltage step is 0,05 V. The SDM nonlinearity for all cases does not exceed the sensitivity of ADC based on appropriate SDM. Therefore the nonlinearity rejection factor of second integrator nonlinearity is more than 5000 (ratio of maximum nonlinearity of integrator to sensitivity of SDM). So the influence of second integrator nonlinearity on SDM nonlinearity is negligible small in comparison with the influence of the first integrator's nonlinearity.

Conclusion. The developed simulation model of single-bit second-order SDM provides independent simulation of all integrators by nonlinear submodels. This model is used to investigate the influence of each integrator nonlinearity on integral nonlinearity of ADC based on this SDM. The results give a possibility to conclude the following:

- the first integrator nonlinearity has a complex character of influence on ADC integral nonlinearity;
- the level of nonlinearity of the second integrator at least 500 times less than the influence on ADC nonlinearity in comparison with influence of first integrator nonlinearity;
- the maximal value of ADC integral nonlinearity is proportional to nonlinearity level of the first integrator;
- the rejection factor of first integrator nonlinearity by ADC based on single-bit second-order SDM is from 8 to 10.

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ИНТЕГРАЛЬНАЯ НЕЛИНЕЙНОСТЬ ОДНОБИТНОГО СИГМА-ДЕЛЬТА МОДУЛЯТОРА ВТОРОГО ПОРЯДКА

Сун Хайменг[1], Р. Кочан[2], О. Кочан[2], Су Джун[3]

[1] – Колледж Ченгуй Университета Жимей, ул. Юинжианг 185, Ксиамен, 361021, Китай,

[2] – Национальный университет «Львовская политехника»,
ул. С. Бандеры, 12, Львов, 79013, Украина, E-mail: kochan.roman@gmail.com

[3] – Хубейский технический университет, Вухань, 430068, Китай.

Разработана имитационная модель однобитного сигма-дельта модулятора второго порядка и аналого-цифрового преобразователя (АЦП) на его базе. С использованием этой модели проведено исследование влияния параметров компонентов на интегральную нелинейность АЦП. Выявлено отсутствие влияния нелинейности второго интегратора на нелинейность АЦП. Библ. 16, рис. 9, табл. 1.

***Ключевые слова**:* сигма-дельта модулятор, интегральная нелинейность, коррекция погрешности.

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ІНТЕГРАЛЬНА НЕЛІНІЙНІСТЬ ОДНОБІТНОГО СИГМА-ДЕЛЬТА МОДУЛЯТОРА ДРУГОГО ПОРЯДКУ

Сун Хаіменг[1], Р.Кочан[2], О.Кочан[2], Су Джун[3]

[1] – Коледж Ченгуй Університету Жімей, вул. Юінжиганг, 185, Ксіамен, 361021, Китай,

[2] – Національний університет «Львівська політехніка»,
вул. С. Бандери, 12, Львів, 79013, Україна, E-mail: kochan.roman@gmail.com

[3] – Хубейський технічний університет, Вухань, 430068, Китай.

Розроблено імітаційну модель однобітного сигма-дельта модулятора другого порядку та аналого-цифрового перетворювача на його базі. З використанням цієї моделі проведено дослідження впливу параметрів компонентів на інтегральну нелінійність АЦП. Виявлено відсутність впливу нелінійності другого інтегратора на нелінійність АЦП. Бібл. 16, рис. 9, табл. 1.

***Ключові слова**:* сигма-дельта модулятор, інтегральна нелінійність, корекція похибки.

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