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ASPECTS OF USING OF SHEET THERMOMIGRATION OF THE Al+Si THREE-DIMENSIONAL LIQUID ZONE TO FORM SEMICONDUCTOR POWER DEVICES

The paper considers using the technology of sheet thermomigration of three-dimensional zones, which implements p^+-Si liquid epitaxy on an n-Si wafer, to produce power semiconductor devices with crystals having thinned layers of high-resistive n-Si base, which are surrounded by p^+-Si* side insulation regions, and thickened p^+-Si* emitter layers. This technology, which has a number of advantages, was used to create diode arrays in n-Si with a specific resistance of 20 Ω·cm. For recrystallization, p^+-Si wafers with a resistivity of 0.005 Ω·cm were used. The produced direct polarity diodes had a breakdown voltage of 1000 V, a forward voltage drop of 1.17 V at a current density of 2.0 A/mm^2, and a reverse resistance recovery time of t_{rr} = 1.5 μs. Additional use of the technology of creation of recombination centers allowed to further improve t_{rr} to 0.5 μs.*

Key words: Al+Si melt, diode, sheet thermomigration, three-dimensional zones.

The development and production of power semiconductor devices (**PSD**) today is guided primarily by the criteria of economy and reliability. Typically, the thickness of the silicon wafers for PSDs is determined by their mechanical strength and durability during the long manufacturing process of the chips. Because of this, both the high-resistance *n*-base of PSD chips and the wafer as a whole have a technological thickness that is difficult to reduce below about 150 μm without losing the necessary technological indicators of mechanical strength and reliability. This means that the high-resistance *n*-base of the structures can often be excessively thick, which is undesirable as regards their optimal parameters. For a number of PSDs used in relatively low-voltage devices, such as those connected to household power networks, this adversely affects some of their parameters. Among other things, it leads to an increase in the direct voltage drop U_F. The thicknesses of near-contact highly alloyed regions, which are formed by diffusion methods, have their own technological thickness limitations and do not allow to radically change both the thickness of the base and the U_F. Such excess can reach 100 μm, which at a current density of more than 1 A/mm^2 leads to noticeable power losses and an increase in the temperature of the device. The reverse voltages U_R required for such PSDs are usually in the range of 500 — 1200 V. Such relatively low U_R values should be matched by relatively low values of the U_F parameter. To ensure appropriate parametric dependences of such PSD structures, there needs to be a technological possibility to reduce the thickness of the *n*-base to 30 — 100 μm, depending on the specific resistance of the original *n*-silicon and the size of the space charge regions of reverse-biased *p–n* junctions. Of course, the requirements for the mechanical durability of the wafers and the manufacturability of the processes remain. Therefore, the decrease in the base thickness must be compensated by a corresponding increase in the thickness of the low-resistance p^+-Si layer of the substrate, which is the anode layer. Also, according to the basic technology, silicon wafers should have a relief surface of 1—3 μm.

Fig. 1 shows two structures formed using different technologies with different base thicknesses. The considered designs of the structures allow both to passivate the rectifier *p–n* junctions and to further control the parameters of the structures with wafers on one side. The structures shown in Fig. 1, *a* were formed using local thermomigration (**TM**) process (or temperature gradient zone melting), where the layers of lateral p^+-insulation, the so-called insulating wall (**IW**), are formed [1—5]. The structures from Fig. 1, *b* were created using the developed sheet TM process, which includes the formation of both the IW layers and a thicker p^+-Si emitter layer, which allows maintaining mechanical properties of the wafers.

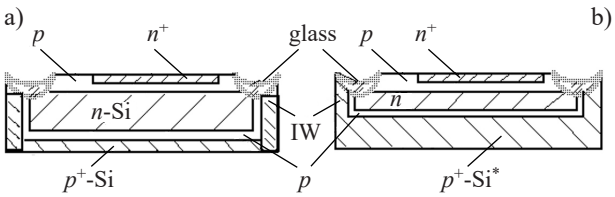

Fig. 1. Thyristor structures created according to the basic technology (*a*) and to the researched technology — with a thinner *n*-Si base layer and a thicker p^+-Si emitter layer (*b*)

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Studies have shown that the flat zone TM is a promising technique for producing PSDs with a thinner *n*-base.

The basis of the researched technology is the TM process, during which the p^+-Si* layers of the substrate and the p^+-Si* IW regions of the chips are created (Fig. 1). The technology also uses grinding processes to reduce the thickness of the semiconductor structure, including the reduction of the thickness of the *n*-base and exposing of the IW layers. This technology makes it possible to obtain structures with reduced UF without deteriorating the values of other important controlled parameters of the devices. At the same time, energy losses are reduced and the temperature regime of the devices is improved. The diameter of such processed wafers can be 100 — 150 mm or more. In this case, TM of 3D zones is an alternative to traditional gas epitaxy. The TM process used in this case is not local, but sheet-like with a liquid recrystallization zone over the entire surface area of the wafer.

The researched technology based on the TM process involves the creation of intermediate structures. To create them, a low-resistance p^+-Si "source" wafer is connected to a high-resistance "working" *n*-Si wafer using Al+Si melt. One of the success factors of this technology is the formation of protrusions on the surface of p^+-Si wafers [3], which form a capillary gap when the wafers are connected. These protrusions make it possible to ensure the same initial thickness of the Al+Si liquid zone of the "*n*-Si — Al+Si melt — p^+-Si" structures during their formation by capillary suction of the melt over the entire surface of the wafer connection.

For PSD chips in the range from 10 to 100 A, it is desirable to use a group technology to expose and passivate rectifier *p–n* junctions from the side of the *n*-silicon surface, as shown in Fig. 1. Such structures can be formed using the investigated technique of sheet thermomigration of Al with internal volumetric three-dimensional liquid zones, which can be abbreviated as sheet TM or 3D TM.

To successfully produce a PSD with thin base using the sheet TM technology, one should start with creating a working wafer — liquid zone — source wafer structure ("*n*-Si — Al+Si melt — p^+-Si"). The movement of the liquid layer of the melt through the gap between the connected wafers under the action of capillary wetting forces forms a liquid zone for sheet TM. The gap capillary consists of a flat part between the wafer surfaces and a relief part with grooves in *n*-Si, which are perpendicular to the wafer surface along the perimeter of the chip. Thus, the liquid zone of the Al+Si melt, which fills the capillaries, is three-dimensional. Later in the process of sheet TM, a layer of recrystallized p^+-Si* is formed on the *n*-Si wafer, and thus the *n*-Si — p^+-Si* structure is created. Moreover, a recrystallized p^+-Si* layer is simultaneously formed both in the region of the topological IW grooves and on the flat horizontal surface of the emitter. The researched technology uses basic technological processes of grinding with a microrelief of 1 — 3 μm, without the use of polishing processes with a high class of surface treatment. Since this method of PSD formation is considered for the first time, is quite appropriate to give a detailed description and analysis of the conditions for its implementation.

This study aims to develop and experimentally verify the possibility of applying the Al sheet thermomigration technology to produce PSDs with a thinner base and thus improved electrophysical parameters.

Literature review

Splicing two silicon wafers or epitaxial deposition of mono- or polycrystalline silicon films in order to obtain thin layers of silicon, including silicon on insulator (**SOI**), is widely used for producing integrated circuits (**IC**). Various technological routes are used to manufacture such structures. One of such routes [6] allows using a technology similar to the one considered in this study.

The method of direct thermal joining of wafers is also used in the manufacture of PSDs. But the structures created using this method are often highly resistive, have an increased defectivity of transition layers and an increased direct voltage drop [7].

The formation of three-dimensional TM zones and their application in manufacturing chips have not been covered in the literature, thus there is nothing to compare with in this particular matter. But there are similar methods and some aspects of this process [1 — 5, 8] that are worth mentioning. The fact is that the speed of zone migration in the temperature gradient field depends on their thickness [1], and there are generally three areas of such dependence. For "thin" zones, migration is to a greater extent determined by molecular-kinetic processes at the "cold" and "hot" boundaries of the zone than by diffusional transport of silicon through the zone melt. This mode was named "kinetic", and the thinner the zones, the lower the speed of their advancement in the temperature gradient field. For relatively "thick" zones, the speed is determined precisely by the diffusion transfer process and practically does not depend on the zone thickness. Of course, there is also an intermediate stage between these two, the so-called mixed mode, where the migration speed does depend on the thickness, but the dependence is negligible. From a technological standpoint, it is the mixed mode that is the most acceptable, because the diffusion mode, despite its advantage as regards the speed uniformity, has a considerable problem of removing the remaining melt after the process is completed.

Adding a third component, such as gallium or tin, to the composition of the zone [9 — 11] is an important factor in increasing stability by equalizing the migrating velocities of liquid zones of different thicknesses. It is reported that the migration stability of the three-component zone is higher than that of the two-component zone, and it is also established that the temperature of the beginning of migration grows with increasing gal-

lium concentration. It is also reported that the migration rate in the thickness range of 10—40 μm varies only slightly, which may serve as an additional advantage of the three-component zones.

Using plasma-chemical method to remove the products of reaction between the zone metal and silicon dioxide after the migration is complete [12] allows expanding the technological possibilities upon completion of the TM process and at the post-migration stage. Migration of zones with different thicknesses is generally undesirable. In practice, this is the reason why the period of proper migration is artificially extended to ensure that the so-called thinned outsider zones reach the finish side of the wafer. Otherwise, you will have to deal with "frozen" zones, which are the root cause of significant mechanical stresses [13—15] and defects. But the latest studies [9—11, 16] allow us to believe that using a three-component zone instead of a binary zone and non-stationary thermal conditions of TM, a zone of regularly variable thickness can move without breaks for a technologically acceptable distance. Non-stationary thermal conditions [16] suggest the presence of a tangential component of the temperature gradient $\nabla T\tau$ (this temperature changes in magnitude and direction over time) with a zero average value, when there is a significant decrease in the difference in the speed of movement of zones with unequal thickness.

The technology studied in this work competes with the technology of creating moderately low-voltage PSDs on epitaxial p^+-n-substrates [13, 14], but, compared to it, has a wider range of resistivity and thickness values of doped layers, while possessing certain advantages in the process of forming deposited layers on the wafer. The sheet TM technology also reduces environmental damage compared to gas-phase epitaxy.

This study does not consider the direct splicing of silicon or bonding the wafers with silicides, because the said methods produce too high a level of electrical resistance in the contact area, and when the operating current flows through the wafer, this leads to a significant increase in U_F and deterioration of the thermal operating conditions of the chip. In addition, these methods are acceptable only for wafers with grinded surfaces, however, when creating PSDs, preference is given to grinded surfaces with microrelief, which is a natural getter.

It is important to note that the researched technology is not a variation of those previously described in the literature, but is a completely independent technology.

Test samples and research methodology

The sheet TM technique based on three-dimensional zones [5] is used to manufacture PSD chips with a thin n-base with peripheral IWs on a thick p^+-Si* substrate. The implementation of the method is explained in **Fig. 2—7**. Before the "n-Si —Al+Si melt — p^+-Si" structures are formed, grooves for the IW are formed on the surface of one of the sides of the n-Si wafer. The other p^+-Si wafer is fitted with microprotrusions [2], which define the width of the capillary gap between the joined wafers. The grooves in the IW region are created using laser scribing, but other methods, such as chemical etching, can also be used (Fig. 2). These grooves will form the insulating side surfaces of the active regions of future semiconductor structures. The depth of the grooves for the IW should slightly exceed the thickness of the n-Si base of the future chip diode. The contact connection of the wafers thus occurs between the surfaces with p^+-Si microprotrusions and n-Si IW grooves. The width of the capillary contact gap, when it is later filled with the Al+Si melt, determines the thickness of the zone in the sheet TM process. The thickness variation of the Al+Si liquid zone during the sheet thermomigration process is determined by the topological microrelief of the grooves on the crystal surface, and the fact that the thicker zones over the depressions of the microrelief move faster allows for epitaxial overgrowth of depressions and leveling of the epitaxial surface relief, which is often necessary when designing semiconductor devices. It should be noted that the microprotrusions on the surface of p^+-Si were successfully formed by both surface etching and local application of films.

During capillary suction, the Al+Si melt fills both the volume of the gap between the wafers and the IW grooves perpendicular to the gap in the n-wafer (Fig. 2). Thus, a three-dimensional liquid zone is created (Fig. 3). This zone can be considered a combination of a flat zone of standard thickness and an ensemble of linear zones of excessive thickness within the IW.

During TM, the three-dimensional zone moves as a whole, changing its shape while moving. As the movement begins in the temperature gradient field ∇T, the zone front (the contact surface of the zone with p^+-Si (Fig. 3) is flat, but when the zones begin migrating, the thicker fragments in the region of n-Si grooves move with a higher speed due to the purely diffusive mode of migration, and thus such areas move forward (Fig. 4). At this stage, the recrystallized p^+-Si* monocrystalline

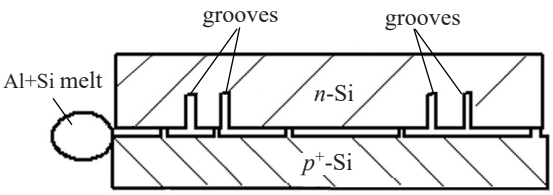

Fig. 2. Initial position of the n-Si and p^+-Si wafers during the liquid zone formation from the Al+Si melt

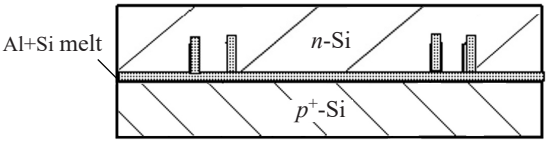

Fig. 3. Formation of the "n-Si —Al+Si melt — p^+-Si" structure necessary to perform the sheet TM process

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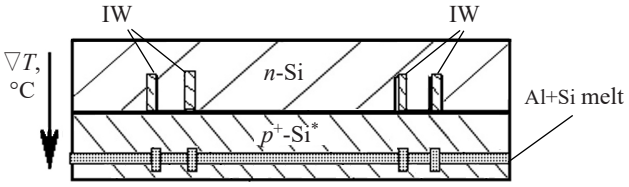

Fig. 4. Modeling of the movement of the three-dimensional zone in the sheet TM during the formation of the p^+-Si*

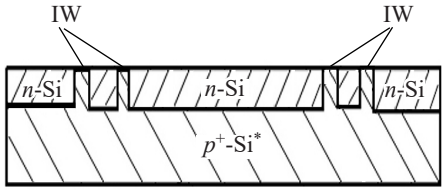

Fig. 5. Creation of a diode matrix during grinding of the p^+-Si*— n-Si structure

regions are formed as a continuation of the single crystal of the n-Si wafer. Moreover, the conductivity of the p^+-Si* region is mainly determined by the conductivity of the original p^+-Si wafer, which has a significant value. Thus a structure with a flat active p–n junction (Fig. 5) and vertical passive p–n junctions of IW layer is formed. Theoretically, if different zone areas move with unequal speed, this can generally lead to the rupture and fragmentation of the zone. The choice of the geometric parameters of the zone and the sheet TM mode should ensure the integrity of the three-dimensional zone as a single complex throughout the entire process. However, the fragmentation of the zone may also be allowed at a significant distance from the planar p–n junction, in the part of the structure that will later be mechanically removed.

It should be noted that both during the formation of the aluminum melt in the volume between the wafers and during sheet TM, Al and B diffuse to the n-Si wafer and the p–n junctions shifts into the volume of the n-Si wafer relative to its surface. At the same time, the formed p–n junctions of p^+-Si* — p^+-Si(n) — n-Si structures are high-voltage. After TM is completed, the obtained p^+-Si*— n-Si structure is mechanically processed. At this stage, IW layers (Fig. 5), which separate high-resistance n-regions and have high-voltage p–n junctions p^+-Si*— p^+-Si — n-Si, are exposed. Thus, a diode matrix is formed on a low-resistance p^+ substrate (Fig. 5). When forming other types of devices, other diffusion or epitaxial regions may be created beforehand on the n-Si wafer.

Different stages of the sheet TM process were carried out on the OH.1944 multi-position installation. The installation has separate chambers for the TM process and for the process of forming structures from wafers connected by an aluminum alloy.

All thermal operations, phosphorus diffusion and oxidation followed a serial route using the necessary pre-diffusion treatments in accordance with the basic PSD technology. Exposing vertical rectifier p–n junctions of the IW by chemical mesa-etching and passivating them with lead-alumino-silicate glass, metallization [2, 5], soldering of diode chips to the metal base, and sealing with plastic were done in the same way as when producing serial diodes in the TO-220 case. Electrophysical parameters of matrix elements, chips and finished diodes were tested in a similar way. Phototemplates, which expose silicon regions in the photoresist mask for subsequent chemical etching of the mesa-grooves, are combined with the IWs placed in the center of the grooves. The parameters of the grooves in the n-type silicon wafer were provided by the current capabilities of the LTU-16 laser.

During the experiment, direct polarity diodes were formed. KDB-0.005 monocrystalline silicon wafers of p-type conductivity with a diameter of 76 mm, a thickness of 500 μm and a specific resistance of 0.005 Ω·cm were used as p^+-Si. KEF-20 n-type silicon wafers were used as n-Si, with a lifetime of charge carriers τ_i of 7.5 μs, a thickness of 330 μm and a diameter of 76 mm. The wafers had a (111) crystallographic orientation, a grinding finish, and underwent standard basic surface treatments. The LTU-16 laser was used to create a grid of double grooves with a distance between the grooves of 200 μm on the "working" wafer. The grooves were cut with a step of 4.55×4.55 mm. The grooves were 40 μm wide and 110 — 120 μm deep. After the grooves were formed, the products of laser cutting needed to be removed. In order to do that, the wafers were treated in a 5% solution of cold KOH alkali until the violent stage of the reaction was complete, after which they were thoroughly washed in hot and cold deionized water.

Along the periphery and in the center of the p^+-Si wafers, columns of Ø1 mm and a height of 25 — 30 μm were chemically etched. This was done to later form a capillary gap between the wafers. Joined together, the p^+-Si and n-Si wafers were fixed in a specialized graphite

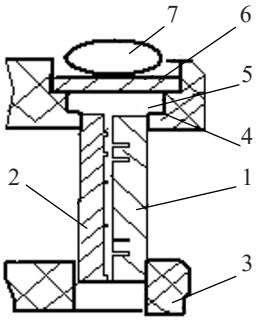

Fig. 6. Schematic of Si wafers fixed in the cassette:
1 — n-Si; *2* — p^+-Si; *3* — lower part of the cassette; *4* — upper part of the cassette; *5* — nozzle; *6* — Si squares for Al+Si melt; *7* — Al solder preform

Fig. 7. Photograph of the upper and lower parts of the graphite cassette used to form "n-Si — Al+Si melt — p^+-Si" structures

cassette. The wafers were installed in the slots of the lower part and fixed with the slots of the upper part of the cassette (Fig. 6, 7). The upper fixing slots were equipped with recesses designed to hold Al and Si samples of a certain mass, and nozzles that direct the flow of the generated Al+Si melt to the capillary gap between the wafers.

The three-dimensional zones were formed by capillary force during wetting of the silicon surface in a vacuum of at least $1 \cdot 10^{-4}$ mmHg at a temperature of 900°C. The material that formed the liquid zone was the A+Si melt with a Si content of 25%. Such a melt was created directly in the process of heat treatment of the cassette with the Al and Si samples. The KOF-70 silicon cut into 7×7 mm squares and high-purity A6N (A999) aluminum were used in the amount necessary to fill the capillary gap. Initially, silicon squares were inserted into the square niches of the cassettes, and the aluminum solder preform was placed on top. When annealing in vacuum began, the components melted together to form the Al+Si melt. Then, when the surface tension forces became insufficient to hold the weight of the Al+Si melt above the nozzle gap with increasing temperature, the melt flowed down the nozzle to the capillary gap. Upon contact with the wafers, the melt was drawn into the gap by capillary forces. Thus, a three-dimensional liquid zone was formed almost instantly.

Apart from the flat capillary, the melt also completely filled the IW grooves in *n*-Si. At this point, the silicon of the wafers began partially dissolving until the equilibrium concentration at the zone formation temperature (37% Si at 900ºC). The bonded wafers were cooled and transferred into another chamber of the TM installation. The OH.1944 installation with resistive heating in a stationary temperature gradient field was described in [2]. The vacuum was at least $1 \cdot 10^{-4}$ mm Hg, and the maximum temperature of the process was 1150ºC. The temperature rose at a rate of up to 100°C/min and cooled by 40—50°C/min.

During grinding, the position of the *p–n* junctions was controlled on the sections along the wafer edges. The cut layers were contrast stained when processed in hydrofluoric acid with the addition of nitric acid.

First, the finish side of the wafer, i.e. the p^+-Si^* layer, was ground until the surface was made plane-parallel. After that, one-sided or two-sided grinding was used to adjust the thickness of the base of the diode matrices to the required thickness (about 100 μm) (Fig. 5). The p^+-Si^* IW was contrast stained to carry out photolithographic alignment.

During phosphorus oxidation and diffusion, the *p–n* junction somewhat shifted towards the region of bulk *n*-type silicon. In total, the high-temperature treatments affecting the displacement of the *p–n* junction lasted about six hours.

Chemical etching of the grooves in the region of rectifier *p–n* junctions of the diode elements, glass passivation of the grooves, and nickel metallization of the contact surfaces were made according to the standard diode manufacturing technology. At the same time, the depth of the mesa-grooves was decreased to 50—60 μm, compared to the regular production technology. This could have been the reason for some permissible decrease in U_R values. Each cathode contact had a metallization area of 10 mm^2. A serial set of phototemplates designed to create diodes with a reverse breakdown voltage U_R at the level of 1.6—2.5 kV was used.

DLS-82E spectrometer was used to study deep level spectra using non-stationary capacitive spectrometry techniques.

Experimental results

Fig. 8 presents the photographs of the investigated *n*-Si — p^+-Si^* structures. Fig. 8, *a* shows the surface of the finish side of the recrystallized p^+-Si^* layer immediately after the sheet TM process. In some areas, e.g., in the lower part of the wafer (Fig. 8, *a*), flat zones do not reach the surface. Fig. 8, *b* shows the surface of the cross-section of the wafer structure with p^+-Si and *n*-Si layers, where extension lines indicate the p^+-Si^* IW insulating protrusions. The p^+-Si^* layers of the substrate and IW changed their color to a darker shade during contrast staining, while the light shade of *n*-Si remained unchanged. The grinded surface of the *n*-Si diode matrix is shown in Fig. 8, *c*, where the double dark lines of p^+-Si^* IW layers visibly stand out on the gray background of *n*-Si.

The image of the unground p^+-Si^* layer shows that the IW (double grid) with a greater zone thickness surfaced completely, while the flat parts of the p^+-Si^* three-dimensional zone did not reach the surface in some areas (Fig. 8, *a*).

This did not affect the functionality of the device, and the possible formation of such structures had been

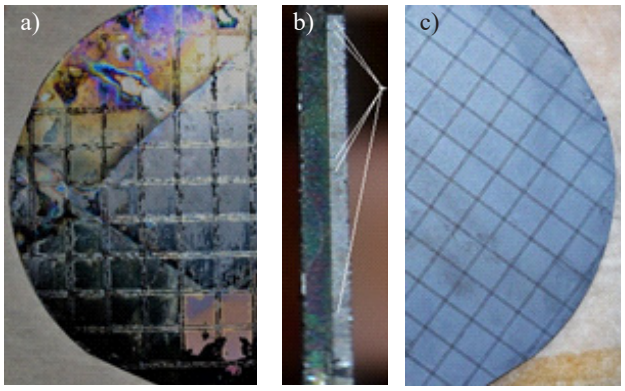

Fig. 8. Photographs of the structures obtained by sheet TM:
a — surface of the recrystallized p^+-Si^* layer before grinding;
b — cross section of *n*-Si and p^+-Si^* layers;
c — *n*-Si surface after grinding

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predicted earlier when analyzing the kinetics of the movement of the studied three-dimensional zones in the sheet TM process.

Analysis of the parameters of the obtained devices

Si wafers with fully formed semiconductor structures of direct polarity diodes are shown in **Fig. 9**. Before dividing the wafer into chips, we tested the reverse voltage U_R of each element, where the reverse leakage current was below 10 μA. The lifetime of minor charge carriers τ_i was measured selectively and found to be 3.2 ± 0.25 μs.

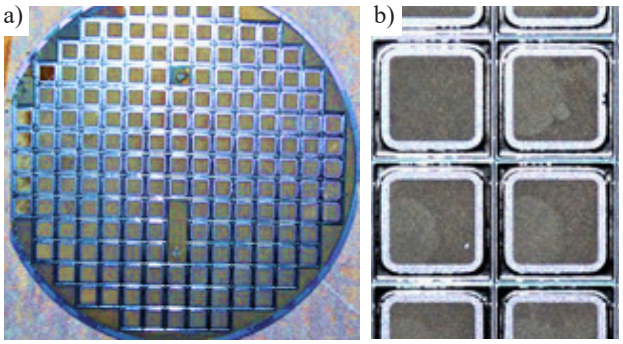

Fig. 9. Full-size (*a*) and enlarged (*b*) photographs of the wafer with diode structures formed by sheet TM and with layers of metallization and insulating glass

Compared to the initial lifetime on *n*-wafers $\tau_i \leq 7.5$ μs, the obtained value can be considered acceptable, considering that no special annealing was done to improve τ_i.

The obtained diode chips had a reverse breakdown voltage U_R at the level of 0.95 — 1.05 kV, which is slightly less than the maximum breakdown voltage of the *p–n* junction for the obtained semiconductor structures based on *n*-Si wafers with a resistivity of 20 Ω·cm. Lower values of U_R were observed in the elements located closer to the center of the wafers. This difference can be explained by a certain curvature of the *n*-Si surface and a decrease in the thickness of the base in the region of the bulge in the center of the wafer during its flat-parallel grinding.

After dividing the wafer into separate chips, the standard technology was used to create diodes in TO-220 case. The resulting diode devices had a reverse recovery time τ_{rr} of about 1.5 μs. This value of the τ_{rr} parameter matches the parameters of some of the standard-technology fast-recovery diodes. The value of the direct current I_F and the corresponding average values of the forward voltage drop $\bar{U}_F$ of the forward polarity diodes are shown in the **Table**. The average forward voltage $\bar{U}_F$ was calculated for groups of 20 diodes. The table also shows the values of the root mean square deviation σ, which are given in millivolts and in relative percentages and demonstrate a slight variation of the U_F values. This indicates high reproducibility of the results. Compared to the mass-produced devices, the diode in the exposed state demonstrates better, lower values of the voltage drop. Irradiation of the studied structures with high-energy electrons [18] allows obtaining τ_{rr} below 500 ns, where $U_F \leq 1.55$ V. Such parameters are significantly better in comparison with the parameters of the mass-produced fast-recovery diodes of this type. Using both the initial *n*-Si with higher values of τ_i and the phototemplate with a larger area of cathode metallization, namely 12.0 mm^2 instead of 10.0 mm^2, will further reduce U_F.

The serial D106 diodes produced by standard diffusion technology with the IW created using local TM of linear zones have $\bar{U}_F$ of 1.22 to 1.27 V at a current of 20 A. For such diodes, τ_{rr} is around 10 μs at τ_i = 20 — 40 μs. Compared to standard diodes, structures made using sheet TM of three-dimensional zones allow switching a larger amount of current, have a lower direct voltage drop and, accordingly, a lower level of losses, while the τ_{rr} parameters allow defining them as fast-recovery diodes of certain frequency groups [18]. The same applies to thyristor chips with optical or electrical control. The obtained results on manufacturing and testing such diodes and thyristors in welding equipment allow talking about the prospects of using them to produce devices powered from 220 and 380 V supply networks. The use of sheet TM allows forming emitter layers with different concentrations of impurities, thereby implementing different types of *p–n* junctions, which is determined and easily adjusted by choosing the value of the resistivity of the original silicon of the p^+-Si wafer for sheet TM. The technology, having a small environmental stress, is able to compete with traditional gas epitaxy, including in terms of increasing the range of breakdown voltage U_R, improving frequency properties and other technical capabilities.

Since the studied technology applies thermomigration liquid epitaxy deposition on a Si relief, it is important to compare it with gas-phase epitaxy on a similar relief.

Direct voltage drop U_F in the structures obtained by sheet TM depending on the amount of direct current

I_F, A	10	12,5	16	20	25	40	50	63	80
$\bar{U}_F$, B	1,02	1,07	1,12	1,17	1,23	1,42	1,52	1,71	1,88
±σ, mV	12	25	20	50	50	70	87	100	90
±σ, %	1,2	2,3	1,8	4,3	4,1	4,9	5,7	5,8	4,8

When considering the gas-phase epitaxial deposition on the relief surface of Si wafers, it is necessary to note that a higher rate of deposition of the Si layer on the surface than at the bottom of the slits may lead to the formation of macrostructural defects, such as volumetric voids deep in the slits. In this case, the application of gas-phase epitaxy on the topological relief may not be appropriate. With some other technologies, for example, the formation of structures with dielectric insulation, the use of gas-phase deposition of thick polycrystalline silicon layers on the relief may lead to significant mechanical stresses, and thus to bending and warping deformation of the wafers.

The studied technology does not exhibit any formation of volumetric overgrowth defects in the slits. At the same time, the monocrystalline silicon layers, both near the grooves with a width of 40 μm and a depth of 120 μm, and on the grinded surface of *n*-Si in the area with a microrelief height of 1—3 μm, are of high quality. The Al+Si melt, both during the filling of the capillary between the joined wafers, and during the start of the sheet TM process, dissolving Si of the surface layers of the microrelief, is saturated with silicon to an equilibrium concentration. The process of dissolution of Si also occurs in topological slit grooves, which are quickly and efficiently filled with the Al+Si melt due to capillary forces. The formation of the solid phase in the volume of the three-dimensional zone occurs as a single coherent front along the entire surface, but with some predominance of the crystallization rate of p^+-Si* in the volume of topological gaps, because the liquid zone of the Al+Si melt is much thicker. Such features of the deposition kinetics in general determine the quality of the formed structures of recrystallized silicon p^+-Si* on the *n*-Si relief. The occurring mechanical stresses are relatively minimal and are to do with the issues of compatibility between the layers with different thermal expansion coefficients. These include the presence of contact of the *n*-Si crystal with the melt zone and the solid phase of the Al+Si melt at different stages of the TM sheet process, as well as the compatibility of the layers with various impurities, respectively P and Al and B. As a result, mechanical stresses may manifest themselves between the layers of p^+-Si* and layers of the *n*-Si wafer in the form of structure bending with convexity on the *n*-Si side. But in the studied technology, there are no layers with mechanical stresses and crystallographic defects similar to those formed on the peripheral surfaces of the IW boundary during local TM in silicon [13, 14]. Such Si layers with different stresses exhibit different kinetics of chemical etching, which is reflected in the formation of a characteristic relief in the process of chemical etching of grooves in the places of deposition of a layer of insulating low-melting glass above the IW. The high level of electrophysical parameters indicates the high quality of the *n*-Si — p^+-Si* interface and of the *p*–*n* junction in *n*-Si.

One of the factors that reduce τ_{rr} of the obtained structures can be the formation of recombination centers (**RC**), which additionally improve the frequency properties of the semiconductor structures of the devices. In this work, the deep-level transient spectroscopy (**DLTS**) allowed revealing the appearance of RCs on the samples described in work [2] during local Al TM and post-operational annealing at a temperature of 1150°C for 4, 9, and 16 hours during the formation of the IW from p^+-Si. The annealing quality was evaluated by the reverse breakdown voltage. On the samples where the annealing time was 4 hours, recombination centers with the energy level $E_{a5} = 0.28$ eV were observed. The indicated centers were not observed in the samples annealed for 9 and 16 hours. The obtained TM RC peaks are similar in shape, but shifted to the region of higher ionization temperatures relative to the $E_{a4} = 0.35$ eV peaks of modified divacancies, which were observed in the spectra of the structures after irradiation with high-energy electrons and low-temperature annealing [18]. It is clear that it is not yet possible to generalize the appearance of such RCs on the structures created by sheet TM based on silicon with different conductivity and different base thickness, and the issue requires further study.

The studied structures surpass the basic ones, such as KEF40, due to the advantages in frequency properties, a thinner base (about 100 μm instead of 160 μm), a higher doped silicon they are made of, and certain technological features of the p^+–*n* junction formation processes.

The impact of the latter can be detailed by comparing it with the parameters of similar epitaxial p^+–*n* structures with the same *n*-Si type formed by standard gas epitaxy technologies. Fast-recovery samples created from these structures have a τ_{rr} value of 0.9 — 1.0 μs. This means that they have better frequency parameters compared to the silicon samples with a higher bulk resistance, but are inferior to the samples created by the sheet thermomigration technology. A feature of the DLTS of such diode samples made of more highly doped silicon is a higher recombination centers concentration. This proves that some improvement of the τ_{rr} parameter in the tested samples occurs due to the formation of recombination centers in the process of performing sheet TM.

Let us consider what can cause the formation and increase in the concentration of RCs. When the Al+Si melt fills the capillary gap between the semiconductor wafers, there begins the process of dissolution of Si atoms in the melt, including on the surface of the relief layer of the *n*-Si wafer. On the surface, in places where Si atoms are extracted, vacancies are formed. These vacancies are partially filled with atoms, mostly silicon and aluminum, partially diffuse into the volume of the basic

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regions of the structures, and all the while they interact, forming divacancies, among other things. Also formed are the connections with various defects, including Si crystal growth defects. Such RCs as divacancies, which are created during local or sheet TM processes, can be considered high-temperature defects. The concentration of such RCs in the samples obtained by sheet TM is significantly greater due to the fact that the surface area of vacancy formation in sheet TM is $2 \cdot 10^4$ greater than in local TM. Another feature of sheet TM is the absence of compressive mechanical stresses at the boundary, which are characteristic of local TM. On the contrary, since the wafer compositions cool down with the melt in their volume, just at the stage of formation of the said RCs, the process is accompanied by the formation and influence of tensile stresses. This feature also causes an increase in mobility, an increase in the concentration of vacancies that diffuse into the volume of the base. The combined effect of these factors may increase the RC concentration, and thus provide a notable improvement in the frequency properties of the devices.

At the same time when the vacancies form and diffuse, the Al atoms are introduced into the *n*-Si surface layers and their diffusion takes place. During the thermomigration process and subsequent high-temperature operations, along with aluminum atoms, boron atoms also diffuse. Thus, p^+-Si regions and a high-voltage *p–n* junction of emitters and lateral insulation are formed in the *n*-Si region. In our experiment, these areas had a thickness of about 15—20 μm at the end of the TM process. The presence of the layers with compressive stresses and defects at the border of the structure created by local TM [2, 8] and their absence in the case of sheet TM leads to differences in the current-current characteristics and breakdown voltages of the corresponding structures. With sheet TM, these characteristics are optimal without additional annealing. The initial RC concentration provides a τ_{rr} value of 1.5 μs. New RCs, which are formed in the process of irradiation with high-energy electrons and annealing at temperatures of 400—450°C, are added to the initial RCs, which are created during sheet TM at a temperature of 1150°C. At the same time, the total RC concentration increases. Such an increase in the RC concentration causes the resulting, so far most optimal, decrease in τ_{rr} from 1.5 μs to $\tau_{rr}^* \leq 0.5$ μs. It is possible that the further development of technological processes of sheet TM will allow improving both τ_{rr} and τ_{rr}^* of fast-recovery and frequency devices even more.

The low mechanical stress level, the high structural quality of the formed *p–n* junctions, the improved frequency properties make the sheet TM process, including if used on relief surfaces, very promising for application in the manufacturing of both PSDs and other semiconductor devices.

Conclusions

The technology of sheet Al TM with a three-dimensional liquid zone developed in the course of this study is designed to form high-quality highly doped epitaxial layers of p^+-Si* emitters and lateral insulation on a significantly large, 100 μm or more, *n*-Si wafer surface with the possibility of forming devices with a thinner *n*-Si base layer. Structures with a thin base layer created using this technology have better parameters of the direct current drop U_F and the recovery time of the reverse resistance τ_{rr}. D106 diodes created according to the developed technology at a breakdown voltage of 1000 V have a reduced voltage drop of 1.17 V in the exposed state at a current density of 2.0 A/mm^2, and a reverse recovery time of 1.5 μs. Using the structures obtained by the sheet TM method to form fast-recovery and high-frequency PSDs by irradiation with high-energy electrons and low-temperature annealing allows producing devices with improved parameters, including with τ_{rr}^* at the level of 0.5 μs and less. The option of different thicknesses of the Al+Si liquid zone of the sheet thermomigration process is given by the topological microrelief of the grooves on the crystal surface, and the property of the prevailing speed of movement of the zone with a greater thickness in the region of the depressions of the microrelief implements the option of epitaxial overgrowth of depressions and alignment of the relief of the epitaxial surface, which is necessary in many cases when implementing designs of semiconductor devices.

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ОСОБЛИВОСТІ ЗАСТОСУВАННЯ ЛИСТОВОЇ ТЕРМОМІГРАЦІЇ ТРИРОЗМІРНОЇ РІДКОЇ ЗОНИ AL+SI ДЛЯ ФОРМУВАННЯ НАПІВПРОВІДНИКОВИХ СИЛОВИХ ПРИЛАДІВ

В роботі розглядається технологія листової термоміграції (ТМ) тривимірних зон, яка реалізує рідинну епітаксію p^+-Si на рельєфі n-Si, при виготовленні силових напівпровідникових приладів, кристали яких мають потоншені шари високоомної бази n-Si, що по периметру оточені областями p^+-Si* бокової ізоляції, та потовщені шари p^+-Si* емітеру. Тривимірні зони формуються капілярним втягуванням розплаву Al+Si в зазор між пластинами p^+-Si та n-Si та в зазор канавок глибиною 120 мкм та шириною 40 мкм, які сформовані в пластині n-Si. Процес ТМ створює шари p^+-Si*, які в канавках є областями бокової ізоляції, а у плоскій частині n-Si — емітером. За такою технологією, яка має ряд переваг, створено діодні матриці в n-Si з питомим опором 20 Ом·см. Для рекристалізації використовували пластини p^+-Si з питомим опором 0,005 Ом·см. Виготовлені діоди прямої полярності мали напругу пробою на рівні 1000 В, напругу падіння прямої напруги 1,17 В при щільності струму 2,0 А/мм^2 і час відновлювання зворотного опору τ_{rr} =1,5 мкс. Додаткове застосування технології створення рекомбінаційних центрів дозволило поліпшити τ_{rr} — до 0,5 мкс.*

Опція різнотовщинності рідкої зони Al+Si процесу листової термоміграції задається топологічним мікрорельєфом поверхні кристалу, а властивість переважаючої швидкості руху зони з більшою товщиною в області впадин мікрорельєфу реалізує опцію епітаксіального зарощування впадин і вирівнювання рельєфу епітаксіальної поверхні, що є необхідним в багатьох випадках при реалізації конструкції напівпровідникових приладів.

Ключові слова: Al+Si розплав, діод, листова термоміграція, тривимірні зони.

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