ОБЧИСЛЮВАЛЬНІ ПРОЦЕСИ ТА СИСТЕМИ

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Typical structure of a duplicate error correction scheme with code control with summation of weighted transitions

Error correction circuit typical structures are described — majority and duplication structure with control by parity. A new structure of the correction circuit based on duplication with weighted-transitions sum code control is proposed. The code is constructed by weighting the transitions between the adjacent bits in data vectors, numbers from sequentially increasing powers of the number «two», starting from the zero degree. The specified code detects any errors in data vectors, except for errors associated with distortions of all data bits at the same time. The weighted sum code features allow it to be used in the synthesis of error detection circuits. An example of the correction circuit synthesis is given. The experiments results using control combinational circuits MCNC Benchmarks showed that the duplication structure with weighted-transitions sum code control in many cases allows one to obtain lower complexity indicators values of the correction circuits technical implementation than the known structure of majority correction.

Keywords: combinational automation devices, systems with fault detection, systems with error correction in calculations, fault-tolerant systems, duplication, triplication.

In the development of discrete devices and control systems, it is important to endow them with the fault tolerance property, which allows them to be insensitive to incorrectly calculated data in the implementation process [1, 2]. This property is achieved by introducing significant redundancy into the hardware and software of the source technical objects [3]. In the process of practical implementation of discrete devices and control systems, the identification of incorrectly calculated values and their correction are carried out using the reser-

vation methods (fractional and multiple), test and functional diagnostics, time and information redundancy.

Typical structures of systems for monitoring and correcting errors in calculations based on multiple reservation of components are widespread [4]. For example, in the field of control systems in railway transport, structures such as 1oo2, 2oo2 (duplication systems), 1oo2D (duplication system with control of each block), 2oo3 (system with majority error correction) are often used in [5—11]. Such systems use not only reservation of the main computing components, but also the advanced technical diagnostics and comparison and error-correction schemes.

The proposed fault-tolerant structure is advisable to use for combinational automation devices. It is based on duplication with weighted-transitions sum code [12] control and makes it possible to synthesize fault-tolerant devices with less hardware redundancy compared to the structure of majority error correction by hardware redundancy.

The correction schemes typical structures. One of the most common structures is the structure with majority error correction (Fig. 1), in which the source device $F(x)$ is supplemented with two copies (not necessarily identical in hardware or software implementation, but only performing the similar functions [13]). The signals from the same-name outputs of three different devices $F(x)$ are fed to the logical elements of majority error correction (elements «≥2»), which implement the function of choosing the majority (voting):

$$\widetilde{f}_i = f_i^1 f_i^2 \vee f_i^1 f_i^3 \vee f_i^2 f_i^3, \qquad (1)$$

where f_i^1, f_i^2, f_i^3, $i = \overline{1, m}$ are the same-name functions implemented by devices $F(x)$ 1, 2, and 3.

The structure with majority error correction shown in Fig. 1, has significant redundancy and actually makes it possible to mask incorrectly calculated function values. It makes it possible to correct the manifestations of any types of faults that occur in one of the devices $F(x)$. At the same time, it is not possible to identify an incorrectly functioning block. This circumstance leads to the need to equip each of the $F(x)$ blocks with a self-checking integrated control circuit [2]. This eliminates the accumulation of faults, which is extremely important for operation as part of control systems for critical technological processes, but further increases the complexity of the technical implementation of the final device.

An alternative kind of implementing a fault-tolerant discrete system is to use a duplication structure with correction and control of calculations by parity (further – «the duplication structure with correction») (Fig. 2). Such a structure is implemented using the $F(x)$ device and its copy, the operation of which

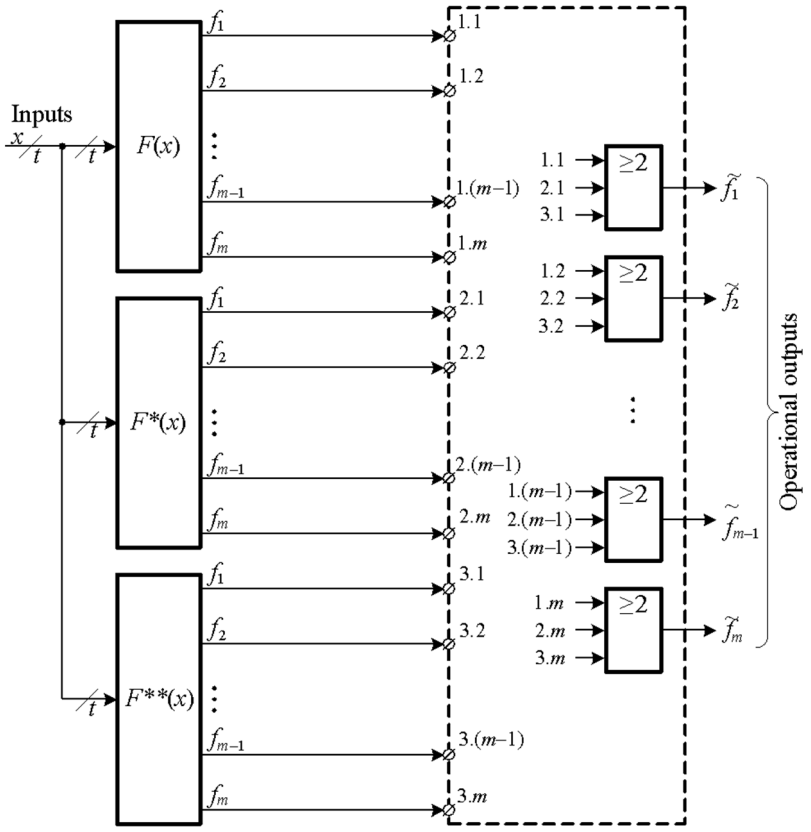

Fig. 1. The majority error correction scheme

is controlled by some attribute, for example, by the parity code [14]. To compare the values at the same outputs of different $F(x)$ blocks, a cascade of two-input adders by modulo two (XOR) is used. If the signals arriving at the inputs of each XOR element are different, then an error signal $e_i=1$, $i=\overline{1, m}$ is generated.

Error signals are received at the first inputs of elements that implement the logical multiplication function. The signal $u = u_1 = u_2 = \ldots = u_m$ from the output of the parity control circuit is fed to the second inputs of these logic elements. In this case, the latter is inverted, because the parity control circuit makes it possible to control the manifestations of faults at the outputs of the copy of the $F(x)$ block. If this is present, it should not be corrected. The correction is implemented directly by the correction circuit, which includes a cascade of logical multiplication elements (AND) with inverters at the second inputs and a cascade of addition elements by modulo two $\alpha_1, \alpha_2, \ldots, \alpha_{m-1}, \alpha_m$.

In the diagram shown in Fig. 2, the correction of any errors that occur at the outputs of one of the $F(x)$ blocks, which are fixed using the parity control

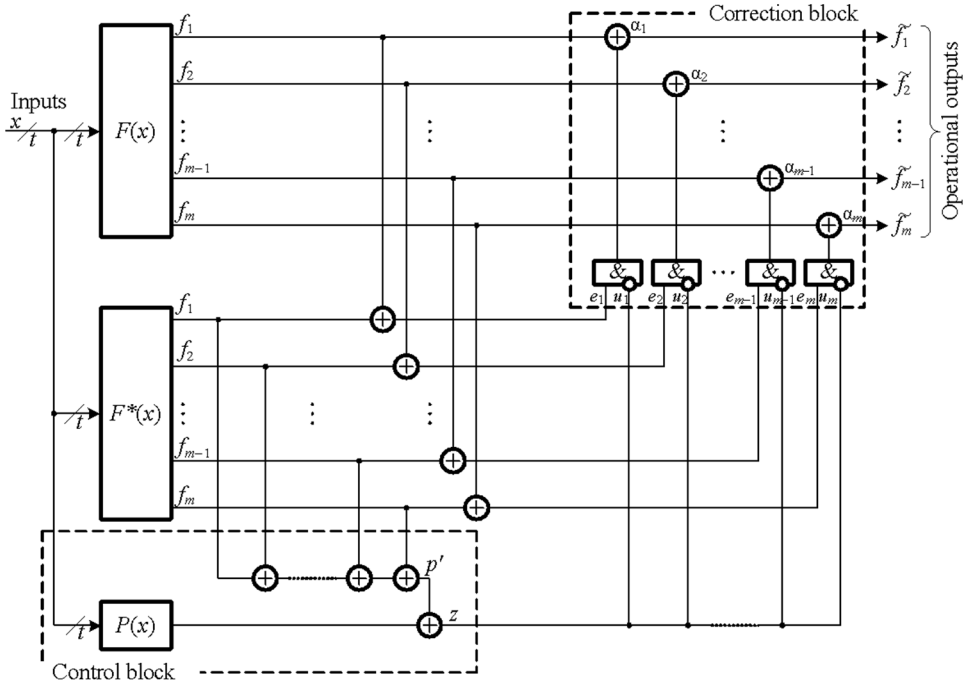

Fig. 2. The duplication scheme with correction and control of calculations by parity

circuit, is performed. In this case, the parity code does not identify errors with even multiplicities [15], and this reduces the probability of error correction in the general case. However, methods of group control of independent outputs [16, 17] or well-known methods of synthesis of devices, the outputs of which form one group of independent outputs [18, 19], can be applied. The use of such methods implies a certain increase in the structural redundancy of devices and leads to a complication of the final system.

The duplication structure with correction does not detect errors in the inputs and outputs of the output cascade of XOR elements. This disadvantage is leveled by the use of highly reliable output comparison elements. It should also be noted that to increase the accuracy of the correction, a duplication structure with double control of the values at the outputs of both $F(x)$ blocks can be applied.

The advantage in the complexity of the technical implementation of fault-tolerant devices with a duplicate correction structure compared to the majority error correction structure can be achieved due to a simpler control scheme than the third copy of the source device.

It should be noted that the structures shown in Fig. 1 and in Fig. 2 are standard. This means that it is constructed using typical blocks, elements, converters, and standard structure optimization tools (for example, the $P(x)$ block in Fig. 2) [12]. This feature provides these structures with a fairly wide application.

Let's consider a modification of the duplication structure with correction by using in the control circuit a redundant code with a larger number of detected errors than in the parity code. This structure is also constructed of standard components using standard structure optimization tools, and it is a typical one.

The error correction schemes structure based on the weighted-transitions sum code. One of the disadvantages of the typical structure of the duplication system with error correction and control of calculations by parity is the impossibility of fixing errors with even multiplicity at the outputs of the checked objects. The number of such errors can be significant. To improve error detection characteristics in checked devices, it is possible to use codes with a large number of detected errors. One of such codes is a code with summation of the weight coefficients of transitions between bits occupying adjacent positions in data vectors (a code with summation of weighted transitions), described in [12].

The rules for this code construction are as follows:

1. The transitions between the bits of the data vector, starting from the lowest bit, are assigned $w_{i,i+1}$ weight coefficients from a series of increasing powers of the number 2:

$$[w_{i,i+1}] = [w_{m-1,m}, w_{m-2,m-1}, \ldots, w_{2,3}, w_{1,2}] = [2^{m-1}, 2^{m-2}, \ldots, 2^1, 2^0].$$

2. The total weight of active transitions is calculated:

$$W = \sum_{i=1}^{m-1} w_{i,i+1} t_{i,i+1},$$

where $t_{i,i+1} = f \oplus f_{i+1}$ is the function for activating the transition between f_i and f_{i+1} bits.

3. The resulting number is represented in binary form and written into the bits of the check vector.

Let's denote the weighted-transitions sum code as $T(m, k)$-code, where m and k are the lengths of data and check vectors. The $T(m, k)$-code has $k = m - 1$ check bits. The check bits values can be determined using the following formulas:

$$\begin{aligned} h_1 &= f_1 \oplus f_2; \\ h_2 &= f_2 \oplus f_3; \\ &\ldots \\ h_{m-1} &= f_{m-1} \oplus f_m. \end{aligned} \qquad (2)$$

To obtain the values of the check bits of the weighted-transitions sum code, only the operations of addition by modulo two are used, therefore the

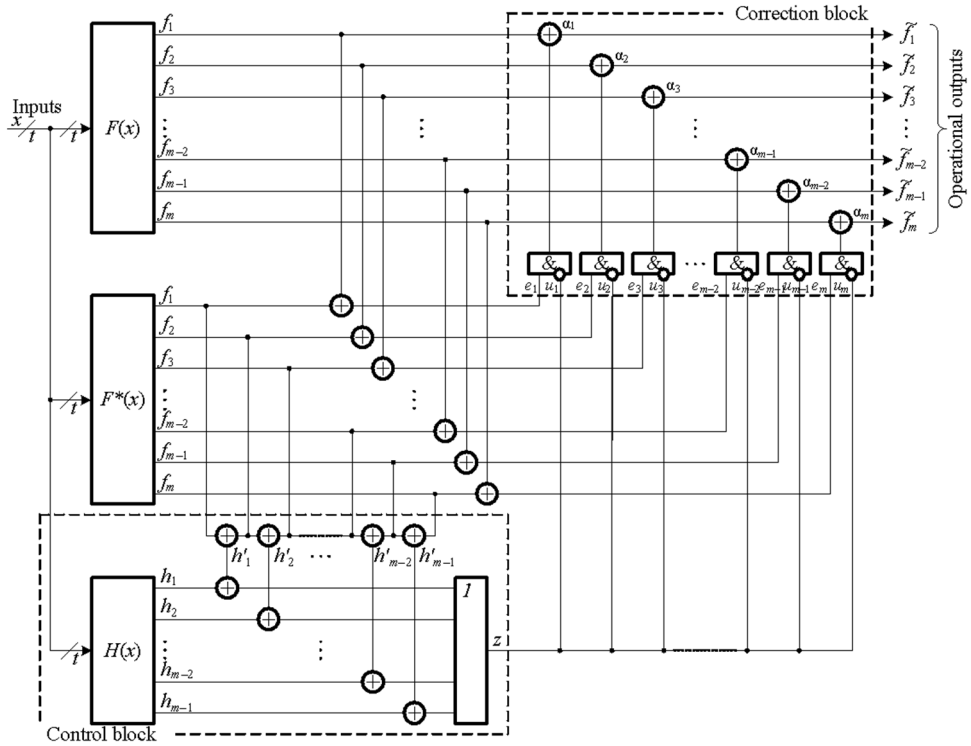

Fig. 3. The duplication scheme with correction and control of calculations by the $T(m, k)$-code

structure of the encoder of this code is standard and contains m–1 element of addition by modulo two. The presence of the standard encoder structure makes it possible to synthesize a typical error correction structure (Fig. 3). The $T(m, k)$-code will detect any distortions in the monitored code vector, except for errors with a maximum multiplicity $d = m$. This is due to the fact that the value of the total weight of the data vector calculated by the formula (1) will not change only if it is calculated for two vectors with completely opposite bit values.

This feature of the $T(m, k)$-code makes it possible to use it very effectively for organizing control of combinational logic devices. At the same time, only one restriction is imposed on the structures of monitored devices – the absence of paths from any internal logical elements leading simultaneously to all their outputs, which can be considered a structural restriction. Even if these elements are present, it is possible to check the exclusion of the simultaneous distortion of all m outputs of the device:

$$\frac{\partial f_1}{\partial y_q}\frac{\partial f_2}{\partial y_q}\ldots\frac{\partial f_m}{\partial y_q}=0, \tag{3}$$

where y_q is a function implemented at the output of the logical element G_q, which is connected by paths to all the outputs of the device. If the expression on the left side of (3) is equal to zero for all such elements, then there is no input set on which errors are transmitted to all outputs of the device.

As indicated in [12], such properties of the T (m, k)-code make it possible to construct a typical structure of the self-checking integrated control circuit called the "almost duplication" structure that can be used as an alternative to the duplication system.

The structure of the correction circuit based on the use of the T (m, k)-code will be called the structure of duplication with correction and control of calculations by the T (m, k)-code, or T-structure. Its advantage in comparison with the well-known duplication structure with correction and control of calculations by parity (Fig. 2) is the ability to fix any errors in the main logic block F (x), with the exception of distortions with a $d = m$ multiplicity. The new error correction structure is less complex than the well-known duplication structure with correction and control of calculations by parity, because it has a large number of functions implemented by the H (x) block. However, the number of identified faults in it is much larger than the duplication structure with correction and with parity control even without modification of the F (x) blocks structures.

Compared to the traditional majority error correction scheme (see Fig. 1), the effect of using the new structure can be achieved by reducing the complexity of one additional device F (x) in the majority correction scheme and replacing it with a control scheme by the T (m, k)-code.

An example of *T*-structure synthesis. Let's consider the goal of a T-structure synthesis for a F (x) device, equipped with four inputs $x_1 \ldots x_4$ and five outputs $f_1 \ldots f_5$, whose operation is described by the truth table (Table 1).

To synthesize a duplication circuit with correction, it is necessary to obtain the formulas describing the outputs of the check bit calculation block H (x). The Table 1 shows the active transitions $(f_i \oplus f_{i+1} = 1)$ for all data vectors, and also determines the summable weight coefficients and the total weight of the W data vector. The W numbers, represented in the binary form, form the $<h_4 h_3 h_2 h_1>$ check vectors.

In the digital devices synthesis, the computer-aided design systems are often used, in which tools for the functions optimizing and assessing the complexity of their technical implementation are integrated [20, 21]. Let's estimate the complexity of the implementation of the structures with the L_{MAJ} majority error correction and the T-structure L_T. For this we will use the well-known SIS interpreter [22]. The F (x) and H (x) blocks were synthesized using SIS and the stdcell2_2.genlib library of standard functional elements using tabular task forms (in the form of *.pla files). The other elements are typical.

Table 1

$x_4x_3x_2x_1$	$f_5f_4f_3f_2f_1$	Active transitions	Weight calculation formula	W	$h_4h_3h_2h_1$
0000	01101	$t_{2,1}$, $t_{3,2}$, $t_{5,4}$	$w_{2,1} + w_{3,2} + w_{5,4}$	11	1011
0001	01110	$t_{2,1}$, $t_{5,4}$	$w_{2,1} + w_{5,4}$	9	1001
0010	10111	$t_{4,3}$, $t_{5,4}$	$w_{4,3} + w_{5,4}$	12	1100
0011	00010	$t_{2,1}$, $t_{3,2}$	$w_{2,1} + w_{3,2}$	3	0011
0100	10110	$t_{2,1}$, $t_{4,3}$, $t_{5,4}$	$w_{2,1} + w_{4,3} + w_{5,4}$	13	1101
0101	00100	$t_{3,2}$, $t_{4,3}$	$w_{3,2} + w_{4,3}$	6	0110
0110	11001	$t_{2,1}$, $t_{4,3}$	$w_{2,1} + w_{4,3}$	5	0101
0111	11001	$t_{2,1}$, $t_{4,3}$	$w_{2,1} + w_{4,3}$	5	0101
1000	11000	$t_{4,3}$	$w_{4,3}$	4	0100
1001	10100	$t_{3,2}$, $t_{4,3}$, $t_{5,4}$	$w_{3,2} + w_{4,3} + w_{5,4}$	14	1110
1010	11010	$t_{2,1}$, $t_{3,2}$, $t_{4,3}$	$w_{2,1} + w_{3,2} + w_{4,3}$	7	0111
1011	01011	$t_{3,2}$, $t_{4,3}$, $t_{5,4}$	$w_{3,2} + w_{4,3} + w_{5,4}$	12	1100
1100	00111	$t_{4,3}$	$w_{4,3}$	4	0100
1101	11111	–	–	0	0000
1110	01000	$t_{4,3}$, $t_{5,4}$	$w_{4,3} + w_{5,4}$	12	1100
1111	00110	$t_{2,1}$, $t_{4,3}$	$w_{2,1} + w_{4,3}$	5	0101

The complexity of the technical implementation of logical devices in SIS is estimated in the conditional indicator of the area occupied by a device on a chip. The following area indicators are obtained for the $F(x)$ and $H(x)$ circuits: $L_{F(x)} = 736$ and $L_{H(x)} = 560$. In this case, the structure of the $F(x)$ device was not changed or optimized (the source device was used). Because the complexity of one majoritarian element is $L_{\geq 2} = 136$, the complexity of the implementation of the majoritarian error correction structure is determined by the value

$$L_{MAJ} = 3L_{F(x)} + 5L_{\geq 2} = 3 \cdot 1080 + 5 \cdot 136 = 3920.$$

Let's determine the complexity of the T-structure implementing. The complexity of the elements of addition by modulo two is $L_{XOR} = 40$. The complexity of the four-input element OR is $L_{4OR} = 48$. The complexity of the element that implements a multiplication function with inversion on one of the inputs, is $L_{AND} = 32$. Taking these data into account, we get the following estimate of the complexity of the T-structure implementing:

$$L_T = 2L_{F(x)} + L_{H(x)} + 18L_{XOR} + 5L_{AND} + L_{4OR} =$$
$$= 2 \cdot 1080 + 560 + 18 \cdot 40 + 5 \cdot 32 + 48 = 3648.$$

The area of the *T*-structure is smaller than the area of the majority error correction structure:

$$\tau = \frac{L_T}{L_{MAJ}} 100\% = \frac{3648}{3920} 100\% \approx 93.06\%.$$

This example demonstrates the effectiveness of using a new structure instead of the classical majority error correction structure.

The experimental results. The experiments were conducted with the control combinational circuits MCNC Benchmarks [23] to evaluate the effectiveness of the *T*-structure application, which used the SIS interpreter and the stdcell2_2.genlib library of functional elements. In the course of the experiment, the structures of the majority error correction, duplication by the correction and with the control of calculations by parity, as well as the *T*-structures were constructed for a number of benchmarks.

The Table 2 shows the results of calculating the areas of the L_{MAJ}, L_T and L_P obtained structures (in conventional units of the stdcell2_2.genlib library). At the same time, the source combinational circuits were not simplified taking into account the selected functional basis, and the $H(x)$ blocks in the *T*-structures were optimized. The τ and π values, given in the Table 2, correspond to the proportion of the area occupied by the *T*-structures from the areas occupied by the structure with the majority error correction and duplication with correction and control of calculations by parity. The π value exceeds 100% for almost all circuits, this is due to the number of control functions calculated in the *T*-structure. It should be noted that in checking calculations by parity without the checked block structure changing, any errors with even multiplicities will not be detected, whereas in the *T*-structure, only errors with the $d=m$ multiplicities will be undetected.

As follows from [24], at the outputs of benchmarks, small multiplicity errors are usually dominated, and their share in the total number of errors decreases as the multiplicity increases. At the same time, the proportion of errors with the $d > 5$ multiplicity is small for the majority of benchmarks (for example, for 5 out of 10 benchmarks it is less than 1% [24, the Table 1]), and errors with maximum multiplicities for the presented circuits do not occur at all [17]. The share of errors with even multiplicity that are not detected during parity control is significant (for 4 out of 10 benchmarks, it was more than 80% of all errors occurring at circuit outputs; for 10 benchmarks, it was more than 50%). The average excess of the *T*-structure area value compared to the duplication structure with correction and with the control of calculations by parity, which is 18.995%, is the price for significantly improved error correction characteristics.

Table 2

Control circuit	$F(x)$	$L_{F(x)}$	L_{MAJ}	L_T	L_P	τ, %	π, %
1	b2	40 952	125 032	108 760	8 7624	86.986	124.121
2	br1	3 608	11 848	11 192	9 048	94.463	123.696
3	br2	2 952	9 880	9 152	7 608	92.632	120.294
4	dc1	976	3 824	3 800	3 120	99.372	121.795
5	dekoder	736	3 104	3 320	2 728	106.959	121.701
6	dist	6 968	21 544	19 360	17 416	89.863	111.162
7	gary	10 688	33 472	34 904	25 440	104.278	137.201
8	in0	10 704	33 520	34 936	25 472	104.224	137.155
9	in1	40 952	125 032	108 760	87 624	86.986	124.121
10	inc	2 376	8 280	8 608	6 560	103.961	131.22
11	intb	22 248	67 640	72 072	96 160	106.552	74.95
12	m1	3 064	10 728	9 936	8 160	92.617	121.765
13	m2	10 096	32 336	26 968	23 240	83.399	116.041
14	m3	13 464	42 440	34 888	30 368	82.205	114.884
15	m4	18 704	58 160	48 520	41 472	83.425	116.995
16	max512	9 632	29 664	25 816	22 688	87.028	113.787
17	max1024	17 816	54 216	47 184	41 392	87.03	113.993
18	mlp4	7 224	22 696	22 432	17 936	98.837	125.067
19	newcpla2	1 896	6 968	6 864	5 680	98.507	120.845
20	newcwp	440	1 960	2 032	1 800	103.673	112.889
21	newtpla2	840	3 032	2 856	2 448	94.195	116.667
22	p82	2 368	8 896	9 160	7 160	102.968	127.933
23	root	3 496	11 128	9 624	8 832	86.485	108.967
24	sqn	2 008	6 408	6 272	5 672	97.878	110.578
25	tms	6 784	22 400	20 344	16 344	90.821	124.474
Average		9639.68	30168.32	27510.4	24079.68	94.614	118.892

Analyzing the τ indicator, we note that for 18 out of 25 benchmarks, a τ value less than 100% was obtained. For 9 benchmarks, the gain in area compared to the majority error correction scheme was more than 10%. On average, the τ indicator value for 25 benchmarks is determined by the value of 94.699%. In this case, the characteristics of the error detection by the *T*-structure are comparable to the characteristics of the error detection with the majority scheme.

The obtained results indicate good prospects for using the *T*-structure for the fault-tolerant combinational circuits synthesis.

Conclusion

The proposed fault-tolerant structure based on duplication with correction and weighted-transitions sum code control of calculations makes it possible to synthesize combinational logic circuits with error correction with less structural redundancy than when using a structure with majority error correction. The gain in technical implementation complexity is achieved by replacing the third set in the majority error correction scheme with a control circuit with reduced implementation complexity. At the same time, the use of the described weighted sum code makes it possible to identify any distortions in the checked block, with the exception of simultaneously occurring distortions of values at all its outputs.

The procedure of the correction scheme synthesizing is quite simple, because the proposed structure is typical. The task of the synthesis is to obtain the $H(x)$ encoder structure of the selected weighted-transitions sum code, described by standard formulas (2), and the other components are selected only taking into account the number of outputs of the source device.

The new error correction structure can be used instead of the majority correction structure for the synthesis of fault-tolerant combinational logic devices.

REFERENCES

1. Shcherbakov, N.S. (1975), *Samokorrektiruyushchiesya diskretnye ustrojstva* [Self-correcting discrete devices], Mashinostroenie, Moscow, USSR.
2. Sogomonyan, E.S. and Slabakov, E.V. (1989), *Samoproverjaemyje ustrojstva i otkazoustojchivyje sistemy* [Self-checking devices and failover systems], Radio & Svjaz`, Moscow, USSR.
3. Gavrilov, M.A., Ostianu, V.M. and Potekhin, A.I. (1969, 1970), *Nadezhnost' diskretnyh sistem* [Reliability of discrete systems], *Itogi nauki i tekhniki. Ser. «Teoriya veroyatnostej. Matematicheskaya statistika. Teoreticheskaya kibernetika»*, 1969, 1970.
4. Sogomonyan, E.S. (2018), Self-Correction Fault-Tolerant Systems, Preprint.
5. Sapozhnikov, V.V., Sapozhnikov, Vl.V., Hristov, H.A. and Gavzov, D.V. (1995), *Metody postroeniya bezopasnyh mikroehlektronnyh sistem zheleznodorozhnoj avtomatiki* [Methods for constructing safety microelectronic systems for railway automation], Transport, Moscow, Russia.
6. Dobiáš, R. and Kubátová, H. (2004), "FPGA Based Design of Railway's Interlocking Equipment", *the Proceeding of EUROMICRO Symposium on Digital System Design*, 2004, pp. 467-473.
7. Dobiáš, R., Konarski, J. and Kubátová, H. (2008), "Dependability Evaluation of Real Railway Interlocking Device", *the Proceeding of 11th Euromicro Conference on Digital System Design*, IEEE Computer Society, Los Alamitos, 2008, pp. 228-233.
8. Chakraborty, A. (2009), "Fault Tolerant Fail Safe System for Railway Signalling", *Proceeding of the World Congress on Engineering and Computer Science (WCECS 2009)*, USA, San Francisco, Vol. 2, October 20-22, 2009.

9. Ubar, R., Raik, J. and Vierhaus, H.T. (2011), Design and Test Technology for Dependable Systems-on-Chip, Information Science Reference, IGI Global, New York, USA.
10. Theeg, G. and Vlasenko, S. (2018), Railway Signalling& Interlocking: 2nd Edition, PMC Media House GmbH, Hamburg, Germany.
11. Borecký, J., Kohlík, M., Vít, P. and Kubátová, H. (2016), "Enhanced Duplication Method with TMR-Like Masking Abilities", *the Proceeding of Conference on Digital System Design (DSD)*, 31 August – 2 September, 2016, Limassol, Cyprus, pp. 690-693. DOI: 10.1109/DSD.2016.91
12. Sapozhnikov, V.V., Sapozhnikov, Vl.V., Efanov, D.V. and Dmitriev, V.V. (2017), "New structures of the concurrent error detection systems for logic circuits", *Avtomatika i telemekhanika*, no. 2, pp. 127-143.
13. Kharchenko, V.S. (1992), "Models and properties of multi-alternative fault-tolerant systems", *Avtomatika i telemekhanika*, no. 12, pp. 140-147.
14. Ghosh, S., Basu, S. and Touba, N.A. (2005), "Synthesis of Low Power CED Circuits Based on Parity Codes", *the Proceeding of 23rd IEEE VLSI Test Symposium (VTS'05)*, 2005, pp. 315-320.
15. Sapozhnikov, V.V., Sapozhnikov, Vl.V., Efanov, D.V. and Cherepanova, M.R. (2016), "Modulo codes with summation in concurrent error detection systems. I. Ability of modulo codes to detect error in data vectors", Elektronnoye Modelirovaniye, Vol. 38, no. 2, pp. 27-48.
16. Gessel', M., Morozov, A.A., Sapozhnikov, V.V. and Sapozhnikov, Vl.V. (1997), *"*Investigation of combinational self-checking devices with independent and unidirectionally independent outputs", *Avtomatika i telemekhanika*, no. 2, pp. 180-193.
17. Sapozhnikov, V.V., Sapozhnikov, Vl.V. and Efanov, D.V. (2018), *Kody Hemminga v sistemah funkcional'nogo kontrolya logicheskih ustrojstv* [Hamming codes in concurrent error detection systems of logic devices], Nauka, St. Petersburg, Russia.
18. Sogomonyan, E.S. and Gössel, M. (1993), "Design of Self-Testing and On-Line Fault Detection Combinational Circuits with Weakly Independent Outputs", *Journal of Electronic Testing: Theory and Applications*, Vol. 4, Iss. 4, pp. 267-281. DOI:10.1007/BF00971975
19. Morosow, A., Sapozhnikov, V.V., Sapozhnikov, Vl.V. and Goessel, M. (1998), "Self-Checking Combinational Circuits with Unidirectionally Independent Outputs", VLSI Design, Vol. 5, Iss. 4, pp. 333-345. DOI: 10.1155/1998/20389
20. Hahanov, V.I., Hahanova, I.A., Litvinova, E.I. and Guz,' O.A. (2010), *Proektirovanie i verifikaciya cifrovyh sistem na kristallah* [Design and verification of digital systems on chips], Novoe slovo, Kharkiv, Ukraine.
21. Harris, D.M. and Harris, S.L. (2012), Digital Design and Computer Architecture, Morgan Kaufmann, USA.
22. Sentovich, E.M., Singh, K.J. and Moon, C. (1992), "Sequential Circuit Design Using Synthesis and Optimization", *the Proceeding of the IEEE International Conference on Computer Design: VLSI in Computers & Processors*, October 11-14, 1992, Cambridge, MA, USA, USA, pp. 328-333. DOI: 10.1109/ICCD.1992.276282
23. "Collection of Digital Design Benchmarks", available at: http://ddd.fit.cvut.cz/prj/Benchmarks/ (accessed September 09, 2020)
24. Sapozhnikov, V., Efanov, D., Sapozhnikov, Vl. and Dmitriev, V. (2017), "Method of Combinational Circuits Testing by Dividing its Outputs into Groups and Using Codes, that Effectively Detect Double Errors", *the Proceeding of 15th IEEE East-West Design & Test Symposium (EWDTS`2017),* Novi Sad, Serbia, September 29 – October 2, 2017, pp. 129-136, DOI: 10.1109/EWDTS.2017.8110123

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ТИПОВА СТРУКТУРА СХЕМИ КОРЕКЦІЇ СИГНАЛІВ
НА ОСНОВІ ДУБЛЮВАННЯ З КОНТРОЛЕМ
ПО КОДУ З ПІДСУМОВУВАННЯМ ЗВАЖЕНИХ ПЕРЕХОДІВ

Описано типові структури схем корекції— мажоритарна і структура дублювання з контролем за паритетом. Запропоновано нову структуру схеми корекції на основі дублювання з контролем по коду з підсумовуванням зважених переходів, який побудовано за допомогою зважених переходів між розрядами, що займають сусідні позиції в інформаційних векторах. Вказаний код виявляє будь-які похибки в інформаційних векторах за винятком похибок, пов'язаних із спотворенням всіх інформаційних розрядів одночасно. Особливості зваженого коду з підсумовуванням дозволяють застосовувати його при синтезі схем виявлення похибок. Наведено приклад синтезу запропонованої нової схеми корекції. Результати експериментів з використанням контрольних комбінаційних схем MCNC Benchmarks засвідчили, що структура дублювання з контролем по коду з підсумовуванням зважених переходів у багатьох випадках дозволяє отримати менші значення показників складності технічної реалізації схем корекції, ніж відома структура мажоритарної корекції.

К л ю ч о в і с л о в а: комбінаційні пристрої автоматики, виявлення несправностей, системи корекції похибок в обчисленнях, відмовостійки системи, дублювання, мажоритарний принцип контролю.

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