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MAGAMP POST-REGULATOR SMALL SIGNAL MODELING

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Abstract. The current paper shows a derivation of MagAmp regulator control loop small signal model. Corresponding simulation results are reported.

Keywords: high-frequency magnetic amplifier, rectangular hysteresis loop, control circuit, small signal model.

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INTRODUCTION

The appearance of high-frequency amorphous alloys with a rectangular hysteresis loop has led to the development of power converters based on high-frequency magnetic amplifiers (MagAmp) with the range of output powers from tens of watts to kW units [1,2]. Due to such advantages as high quality output voltages, high level of dynamic characteristics, high radiation and mechanical resistance, low level of electromagnetic interference, high level of reliability and efficiency, they have found their application in various fields - space, medicine, radar, transport, communications, information technologies, nuclear energy, etc. [3]. Their feature is the extreme simplicity of the MagAmp control scheme. Mathematical modeling and simulation of MagAmp post regulator is carried out in this article.

1. A Quick Review of MagAmp Post-Regulator.

MagAmp switch is just a coil wound on a core with a relatively square B-H characteristic as shown in Fig. 1. The MagAmp is operated in two operating regions, either along the steep or along the shallow slopes of the B-H curve [4]. In the vicinity of operating point *R* the MagAmp core is unsaturated. Here, the high permeability of the core causes the MagAmp winding to present a high inductance to the circuit, which allows only a trace current to flow. MagAmp requires a certain volt-sec, which is the integral of voltage over time, to be applied to its terminals for the magnetic flux to build up in the core and reach the saturation level. The stronger the reset field, the more volt-secs the MagAmp can withstand until saturated. Once saturated, MagAmp operating point shifts to *L*, see Fig. 1. Here, the permeability of the core is very low and the inductance of the MagAmp coil has only a negligible value, which allows a large current flowing in the circuit.

A MagAmp can be used as a semi controlled switch that can block and delay the applied voltage. However, MagAmp cannot interrupt the current once started. Hence, MagAmps are used in pulse circuits where they are assisted by diode rectifiers, which cut off the current as the applied voltage changes polarity.

Here, the MagAmp post-regulator is implemented as a push-pull full-wave circuit [5] at the secondary of the power transformer, T, as shown in Fig. 2. The post-regulator is comprised of a pair of the MagAmp switches SR1 and SR2; power rectifier diodes D1-D2; a free-wheeling diode D_{FW} and a second order LC output filter.
As compared to a single ended MagAmp circuit, the push-pull MagAmp configuration has the advantages of the symmetrical operation and doubled dc output voltage.

Here, both MagAmp switches operate with current reset. The reset current, I_R, is provided by the controller as discussed below. The steering diodes D_{R1} and D_{R2} naturally steer the reset current, I_R, towards the device to be reset. Each MagAmp is wound using two parallel strands of litz wire on the same core. The parallel connection of the MagAmp windings lowers the equivalent resistance of the conduction path and accordingly, lowers the power losses of the power stage under high load current.

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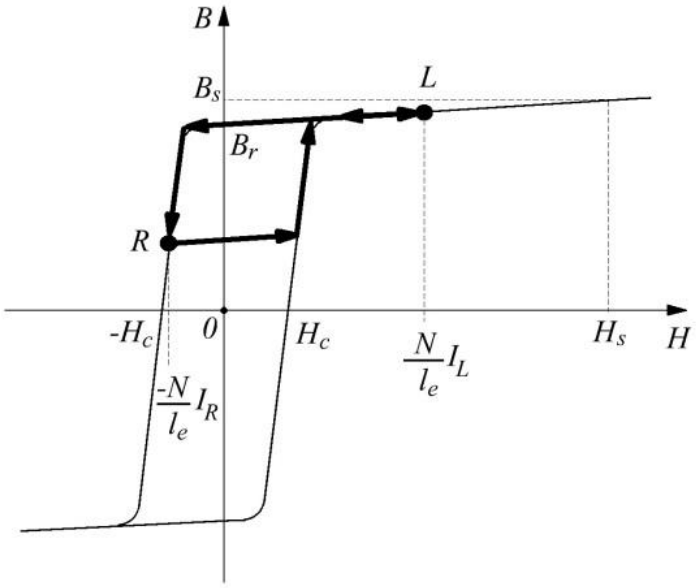


Fig. 1. MagAmp switching trajectory in B-H plain

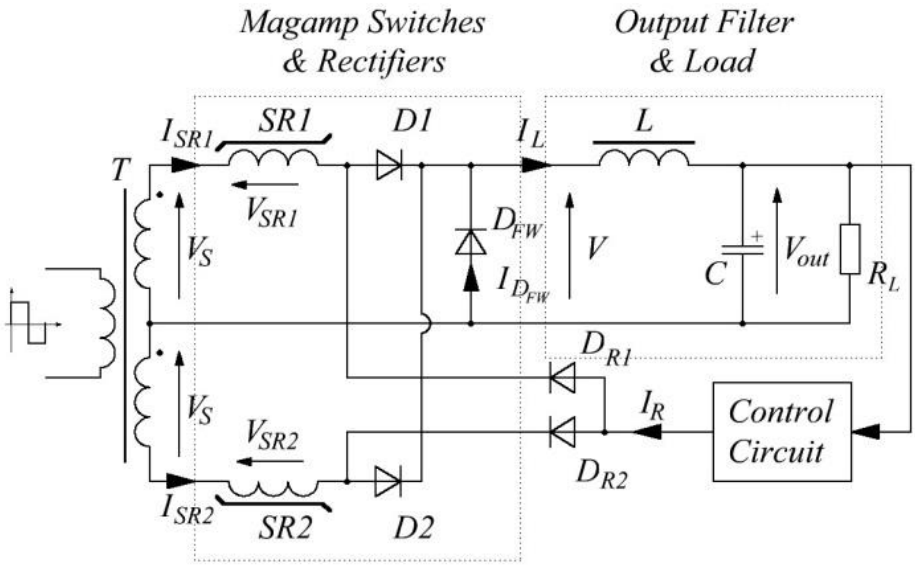


Fig. 2. Push-pull MagAmp regulator circuit

Idealized waveforms of the push-pull MagAmp postregulator are illustrated in Fig. 3. The upper trace is the transformer secondary winding voltage, V_S. The second and third traces show the MagAmp voltages, V_{SR1}, V_{SR2}. The positive portion of the MagAmp waveform represents the volt-secs blocked by the MagAmp, whereas the negative portion of the waveform is due to the reset process. As a result of the MagAmp blocking, the MagAmp output voltage, V, has a reduced duty cycle and, therefore, has a reduced average value. Fig. 6 also shows the output filter inductor current, I_L, and the currents of the MagAmp switches, I_{SR1} and I_{SR2}. The MagAmp blocking state current is drawn out of proportion for illustration purposes. The free-wheeling diode current, $I_{D_{FW}}$, provides the conduction path for inductor current when the MagAmps are in the blocking state.

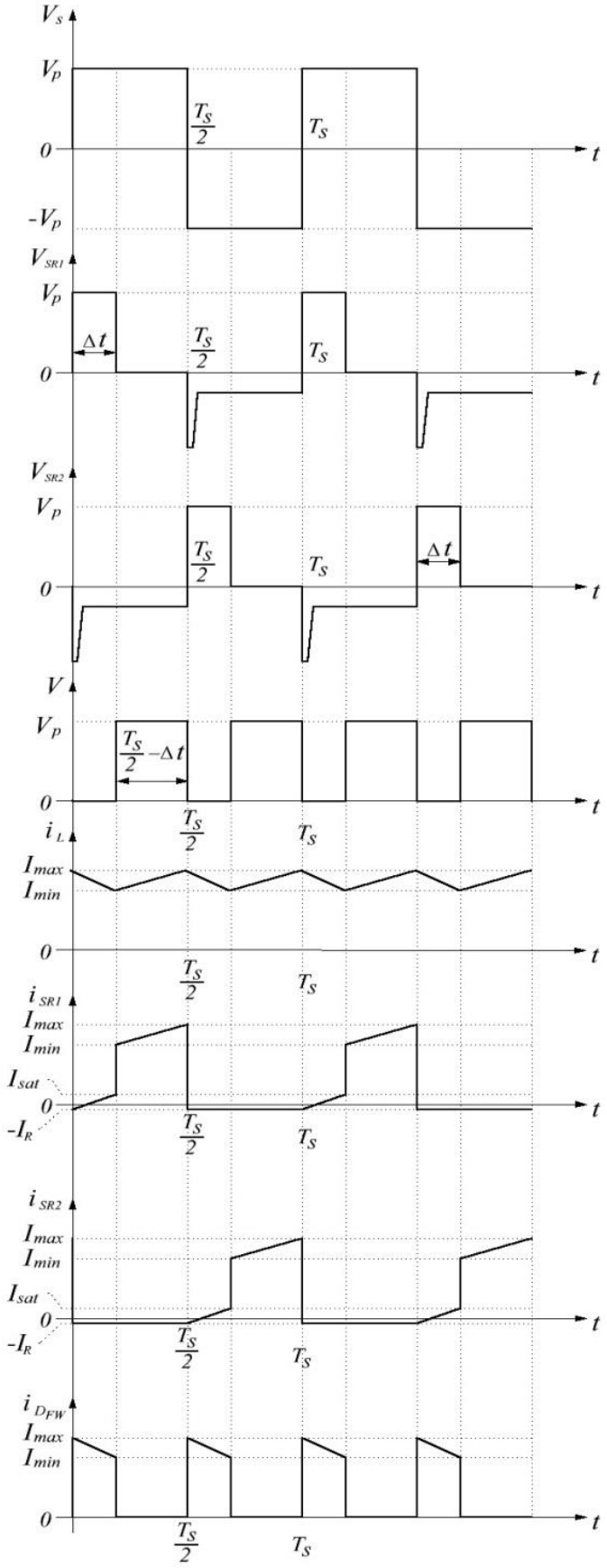


Fig. 3. Waveforms of a push-pull MagAmp regulator

2. MagAmp Control Circuit.

The proposed MagAmp control circuit is shown in Fig. 4. This circuit is a simplification of that used in [6]. The circuit is fed directly by the output voltage, V_{out}. Resistor divider R1, R2 determines the feedback ratio, breakdown diode D8 provides the voltage reference, whereas the PNP transistor Q3 realizes a transconduction error amplifier, G_m. The compensation network is constituted of R_{e1}, R_{e2}, C_e. The collector current of Q3 is applied to MagAmp switches as the reset current, I_R.

Under closed loop action, assuming also that the voltage drop across Re1 is negligible, the converter's steady state output voltage is established according to:

$$V_{out} = (V_z + V_{EBon}) \cdot \left(1 + \frac{R_2}{R_1}\right) \tag{1}$$

Here, V_z iz the breakdown voltage of D8 and V_{EBon} is the ON voltage of Q3 emitter –base junction.

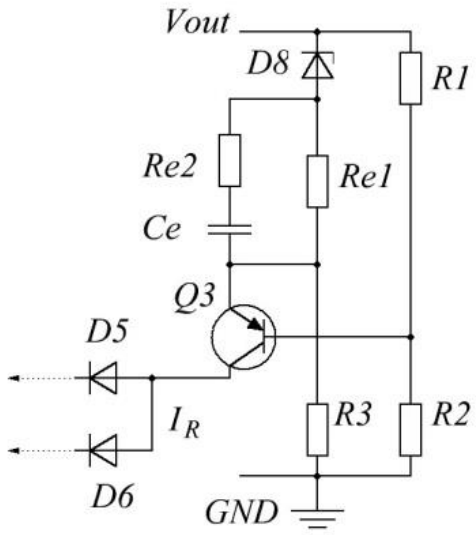


Fig. 4. Control circuit of MagAmp post-regulator

3. Control Loop Small Signal Model.

A simple approximate average large signal behavioral model of the MagAmp switch derived in [7] is presented with equations

$$V_{av} = \frac{2}{T_s}(V_p T_{on}) = V_p - 2 f_s L_{SR} I_{\max} - 2 f_s L_{SR} I_R = V_{av\max} - 2 f_s L_{SR} I_R \tag{2}$$

where V_{av} is the average voltage applied to the input terminals of the output filter by the push-pull MagAmp stage, $f_s = \frac{1}{T_s}$ is the switching frequency, and $V_{av\max}$, is the maximum average voltage that could be attained with zero reset current:

$$V_{av\max} = V_p - f_s L_{SR} I_{\max} = V_p - 2 f_s N_{ma} A_e B_{\max} \tag{3}$$

Considering the conventions, adopted in this text, and the doubled gain of the push-pull MagAmp arrangement, the model is similar to that derived by [8]. Here, however, the delay of MagAmp and its associated phase lag will

be considered next. More accurate model of MagAmp was derived in [9], [10], however, the relative complexity of those makes it inconvenient to be used by a circuit designer.

The MagAmp controller is implemented entirely on the secondary side of the power transformer and employs a single voltage loop. Average model of MagAmp control loop after [9] is shown in Fig. 5. Here, $H_{ma}(s)$ is the average MagAmp small signal transfer function, $H_d(S)$ is the MagAmp delay transfer function and $H_f(S)$ is the output filter transfer function. The voltage reference, V_{ref}, the feedback, β, the summer and the error amplifier transfer function, $G_m(S)$, are implemented by the controller circuitry.

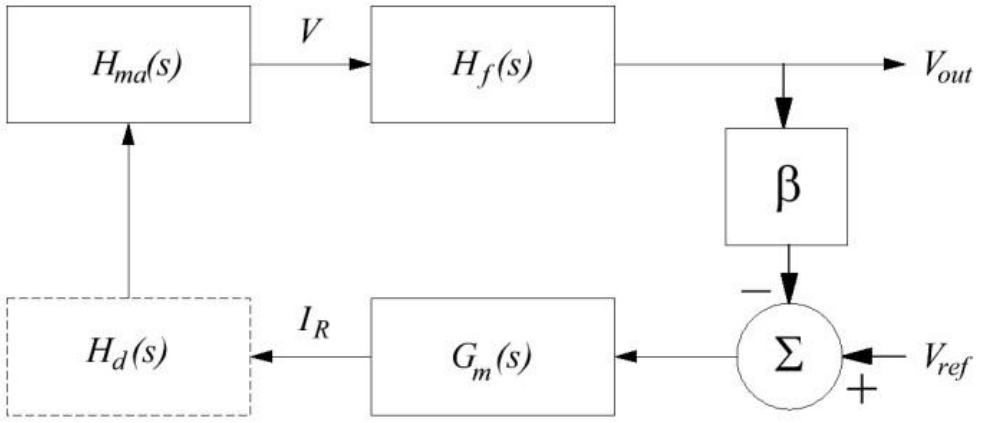


Fig. 5. Average model of MagAmp control loop

$$H_{ma}(S) = \frac{v_{av}}{i_R} = -2 f_s L_{SR} \tag{4}$$

The MagAmp reset during the negative half cycle programs the MagAmp response in the subsequent positive half-cycle. Therefore, the MagAmp response is delayed by half the switching cycle, $\frac{T_s}{2}$. This time delay introduces a phase-lag. First order Pade approximation [11] of the delay transfer function is known to be:

$$H_d(S) = e^{-\frac{T_s}{2}S} \approx \frac{1-\frac{T_s}{4}S}{1+\frac{T_s}{4}S} = \frac{1-\frac{S}{4f_s}}{1+\frac{S}{4f_s}} \tag{5}$$

In the frequency domain the time delay can be expressed as:

$$H_d(jf) \approx \frac{1-j\frac{f}{0.63 f_s}}{1+j\frac{f}{0.63 f_s}} \tag{6}$$

Equation (6) reveals that MagAmp time delay transfer function, $H_d(S)$, has a left half-plane pole and a right half-plane zero which combined effect contributes a 180 degrees of phase-lag at high frequencies. As predicted by (13), the MagAmp phase lag becomes noticeable above $0.063 f_s$, which is a rather low value.

It is also assumed that the post-regulator LC-type output filter has a common second order transfer function given by:

$$H_f(S) = \frac{1}{1 + \frac{1}{Q}\left(\frac{S}{\omega_n}\right) + \left(\frac{S}{\omega_n}\right)^2} \tag{7}$$

where $\omega_n = \frac{1}{\sqrt{LC}}$ is the natural resonant frequency and $Q = \frac{R_L}{\sqrt{L/C}}$. Here, *L* and *C* are the output filter elements and R_L is the load resistance.

The model of MagAmp control circuit of Fig. 4 is shown in Fig. 6a. Here, the small signal T-model was used to represent the PNP transistor Q3. The reference voltage, $V_{ref} = V_z$, represents the Zener diode breakdown voltage. Accordingly, the small signal reset current, i_R, is:

$$i_R = i_C \approx i_E \approx \frac{\beta v_{out} - V_{ref}}{Z_E(S)} = \left(-\frac{1}{Z_E(S)}\right)\left(V_{ref} - \beta v_{out}\right) \tag{8}$$

Equation (8) can be represented by a block diagram as shown in Fig. 6b. In (8) the small signal emitter resistance, r_e, was neglected and the resistor divider ratio is defined as the feedback ratio:

$$\beta = \frac{R_1}{R_1 + R_2} \tag{9}$$

Whereas, the gain of the error amplifier is:

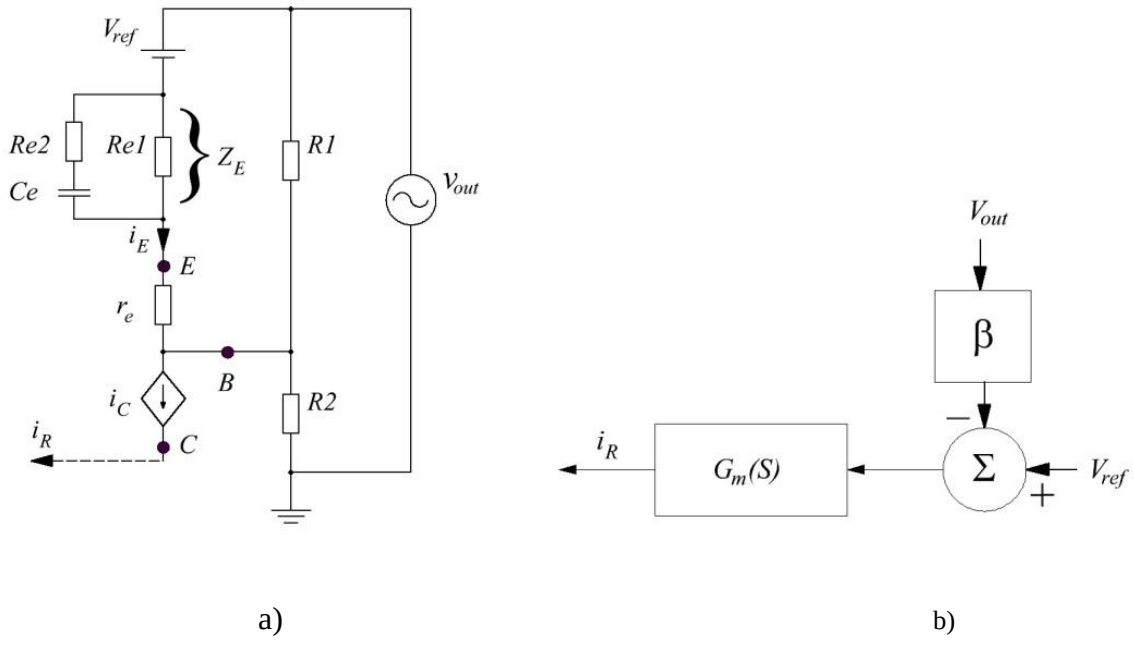
$$G_m(S) = -\frac{1}{Z_E(S)} = \left(-\frac{1}{R_E}\right)\left(\frac{1 + \frac{S}{\omega_z}}{1 + \frac{S}{\omega_p}}\right) \tag{10}$$

The low frequency zero $\omega_z = C_e R_{e1}$ and the high frequency pole $\omega_p = C_e R_{e2}$ are introduced by the compensation network, Z_E.

The resulting MagAmp post-regulator loop-gain, see Fig. 5, is obtained combining (4), (5), (7), (9) and (10) as:

$$G_L(S)=\beta G_m(S)H_{ma}(S)H_d(S)H_f(S)=$$

$$=\left(\frac{R_1}{R_1+R_2}\right)\left(-\frac{1}{R_E}\right)\left(\frac{1+\frac{S}{\omega_z}}{1+\frac{S}{\omega_p}}\right)\left(-2f_sL_{SR}\right)\left(\frac{1-\frac{S}{4f_s}}{1+\frac{S}{4f_s}}\right)\frac{1}{1+\frac{1}{Q}\left(\frac{S}{\omega_n}\right)+\left(\frac{S}{\omega_n}\right)^2} \quad (11)$$



a) b)

Fig. 6. MagAmp controller equivalent circuit a) and its small signal model b)

The loop-gain transfer function (11) has four poles, one right half-plane zero and one compensator zero. Clearly, the loop gain has a substantial phase lag. Also, note that the two minus signs in the expression cancel each other so the loop gain is positive.

In order to stabilize the system the loop crossover frequency should be chosen so that the MagAmp delay has no much effect on the phase. Considering the delay term (6) that is contributed to (11), the loop gain crossover can be designed somewhat lower than MagAmp's delay function pole and zero so that $\omega_c \le 0.4 f_s$. With this choice, the compensator zero is placed at the output filter pole frequency, $\omega_z = \omega_n$, to create a single pole gain roll off in the vicinity of the crossover frequency. Compensator pole should be placed as high as possible. The loop-gain magnitude can be adjusted varying the emitter resistor, R_{e1}. Therefore, to allow acceptable loop gain R_{e1} resistor value should be kept small, up to several tens of Ohms. This also justifies the assumption above used to derive the dc output voltage (2). In the limiting case, when no external resistor is used, R_{e2} is merely the C_e capacitor ESR.

4. Simulation of MagAmp Control Loop.

The frequency response of the MagAmp post-regulator blocks were modeled using PSPICE software and plotted in Fig. 7. The plot clearly shows the MagAmp delay phase lag in effect above 1kHz. The corner frequency of the output filter is about 100Hz. The lead-lag compensation network with phase bump around 300Hz is designed to stabilize the system. The compensated frequency response of MagAmp post-regulator loop-gain $G_L(f)$ is plotted in Fig. 8. The design yielded a stable system with the crossover frequency of 730Hz and phase margin of 45 degrees.

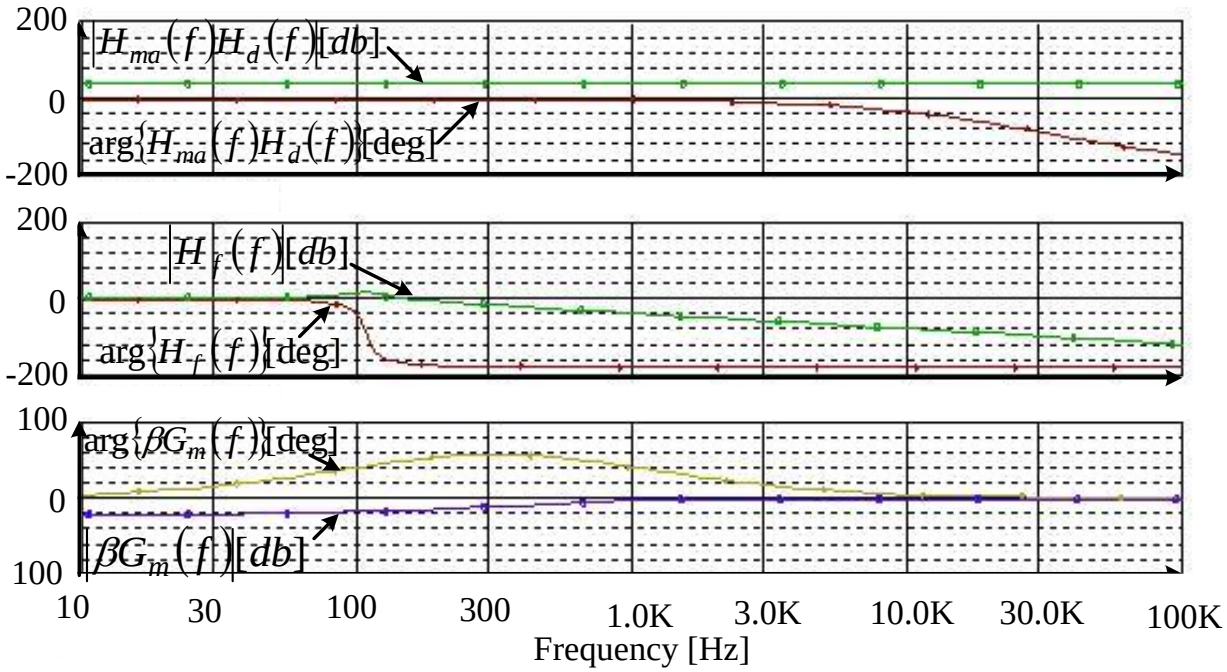


Fig. 7. Simulation results: frequency response of MagAmp post-regulator control loop components. Top trace: MagAmp frequency response including the delay, $H_{ma}(f)H_d(f)$; middle trace: output filter frequency response, $H_f(f)$; bottom trace: control circuit frequency response $\beta G_m(f)$.

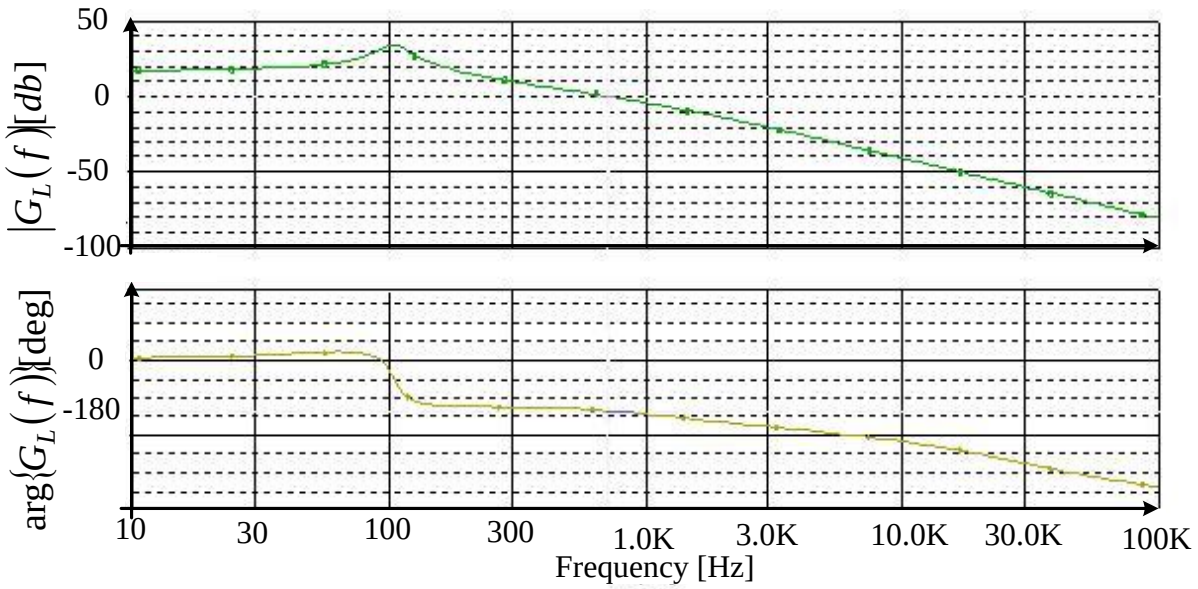


Fig 8. Simulation results: overall frequency response of MagAmp post-regulator loop-gain $G_L(f)$. Top trace: Magnitude [db]; bottom trace: Phase [deg]

Conclusion

The paper proposed a simple MagAmp control circuit. A derivation of the simplified small signal model of the control loop was presented. The suggested model can be used for both theoretical and simulation study. A design procedure was also suggested.

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