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STUDY OF EDDY CURRENT FLAW DETECTOR BASED ON DOUBLE-CIRCUIT SELF-GENERATOR OPERATED IN INTERMITTENT OSCILLATING MODE

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ABSTRACT

Timely application of nondestructive methods for testing critical structures of modern engineering is an important factor ensuring their safe and trouble-free operation. Eddy current testing means have no alternative for contactless detection of cracks in aircraft structures. In order to detect surface cracks (also through a layer of dielectric coating), self-generator eddy current flaw detectors are used, working at operating frequencies above 1 MHz. To develop such flaw detectors, it is promising to use double-circuit self-generator oscillatory system, operating in intermittent oscillatory mode. This work is a study of new technical solutions, in particular self-generator circuit based on a field transistor with insulated gate, circuit of controlling the generation frequency and circuit of regeneration of self-generator oscillations. Their advantages in terms of sensitivity are shown, compared to traditional circuits. The analyzed engineering solutions were used to develop self-generator eddy current flaw detectors of VD 3.03N, VD 3.02N, VD 4.01N and VD 4.03N type for surface crack detection, which have passed state testing and are widely used, in particular for maintenance of SC "Antonov" aircraft and SC "Ivchenko-Progress" and PJSC "Motor-Sich" aircraft engines. It is intended to apply these engineering solutions in the new self-generator flaw detector with functions of automatic adjustment for the level of sensitivity and its indication set by the specified procedure.

KEYWORDS: eddy current nondestructive testing, self-generator eddy current flaw detector, surface cracks, intermittent generation, double-circuit, oscillation regeneration

INTRODUCTION

Reliability and safety of critical structures and components of modern engineering largely depends on timely application of nondestructive testing (NDT) means during their fabrication and operation, which is particularly important under the conditions of extension of service life and operating loads, influence of aggressive media, etc. Means of eddy current NDT using more than 1 MHz operational frequencies have traditionally been used for contactless detection of shallow cracks in metal structures [1, 2]. At the same time, eddy current method has a considerable sensitivity to a range of factors (alongside defects), which influence the eddy current probe (ECP) output signal. Among such factors we will note changes in specific electric conductivity (SEC) and magnetic permeability of the material of the tested object (TO), influence of the edge of the tested object, variation of the geometrical parameters and gap between the ECP and tested object (TO) surface (lift-off effect). Changes of the lift-off and ECP inclination during manual testing are considered to be the most harmful sources of erroneous operation of the testing instrumentation. Changes in the lift-off, caused by different roughness of TO surface or variations of the thickness of the dielectric coating, can also lead to erroneous operation of eddy current flaw detector (ECFD). Therefore, in order to obtain valid results, it is important to ensure a high level of attenuation of the lift-off effect and simple interpretation of testing results.

ECFD of self-generator type are widely used for eddy current flaw detection in structures and components in different industries [1–8]. A common feature of such ECFD is connection of single-coil ECP as an element of oscillatory circuit of self-generator (SG), which is a nonlinear resonance amplifier, included into a feedback loop [9]. Flaw detectors of this type were introduced already in mid-50s of the previous century, which was related to mastering the production of heavy aircraft and powerful aircraft engines [1]. At the end of 80s of the previous century self-generator ECFD of PROBA-5 and TVD-A type were serially produced, and are still operating successfully in some enterprises [1, 3, 4]. Self-generator ECFD are characterized by a high sensitivity to surface-breacking defects, possibility to suppress the lift-off influence, autonomous power supply, small dimensions and weight. Many variants of construction of self-generator ECFD have been proposed, each of which has its shortcomings and advantages. Comparative analysis of different variants of construction and classification of self-generator ECFD is given in work [10].

Oscillatory system of self-generator used in ECFD may consist of one or two resonance circuits. Single-circuit SG were built by the scheme with a common base and capacitive feedback. Double-circuit self-generator have better metrological characteristics due to a more

flexible readjustment into different modes. An important difference of double-circuit ECFD is the dependence of feedback coefficient on frequency that may be used to attenuate the lift-off influence [1, 8, 10, 11]. An important feature of self-generator ECFD also is the type of oscillations produced by the self-generator. In some ECFD models, for instance VD-22N (PROBA-5), permanent continuous oscillations are used [3]. Application of intermittent oscillations looks promising. They are formed under the condition, when the time constant of the automatic bias circuit $\tau_b = R_r \cdot C_s$ (R_r and C_s are the resistor resistance and separating capacitance in the gate circuit) will be greater than the time constant of the working oscillation regeneration $\tau_{osc} = 2L/R$ (L and R are the inductance and resistance of ECP winding), i.e. under the condition of $\tau_b >> \tau_{osc}$ [1, 4, 8, 10]. An additional advantage of such ECFD is the possibility of construction a sound change-tone indication without application of voltage-controlled low-frequency generators. More over, ECFD with intermittent oscillations allow controlling exceeding of the ECP lift-off by ear, due to change-tone indication [4]. The frequency of passage of a series of high-frequency oscillations changes at the change of introduced resistance of ECP, as ECP parameters influence the time constant of the working circuit. Selection of the value of time constant of the automatic bias circuit allows setting the frequency of passage of a series of high-frequency oscillations in the sound range. An additional advantage of ECFD with intermittent oscillations is its cost-effectiveness, as the active element does not consume energy during interrupted generation that is important for ECFD with autonomous power supply. The method to obtain intermittent oscillations is determined by selection of values of *RC*-elements of automatic bias in the transistor gate (base) circuit [1]. The given short overview highlighted the effectiveness of construction of self-generator ECFD on the base of application of double-circuit scheme operated in intermittent oscillating mode [8, 10, 11].

The **objective** of this study is analysis of engineering solutions, invented during development of portable self-generator ECFD of VD 3.03N, VD 3.02N, VD 4.01N and VD 4.03N type (Leotest VD). We are talking about an improved SG scheme, self-generator frequency control circuit (SFCC) and self-generator oscillation regeneration circuit (SORC).

1. DEVELOPMENT AND INVESTIGATION OF AN IMPROVED SELF-GENERATOR SCHEME

Bipolar transistors or field transistors with a closed *p-n*-junction are most often used as an active element in many known self-generator ECFD. Conducted analysis showed that an effective circuit of self-generator ECFD can be based on insulated-gate field transistors, in which the feedback circuit is practically not loaded by active element input resistance (Uchanin V.M., Cherlenevskyi V.V. Eddy current flaw detector. Patent of Ukraine 39207, 2009, Bul. No. 3). The proposed scheme (Figure 1) consists of a double-circuit SG 1, having working loop 2 with connected into it ECP 3 of parametric (single-coil) type and reference loop 7. Self-generator 1 is based on insulated-gate field-effect transistor 9, with diode 6 additionally connected into its automatic bias circuit in parallel to resistor 8. SORC 10 is additionally connected between SG 1 output and power block 12. Sound indication block 11 is connected to the output of SG 1. Varicap 4 can be connected into SG working circuit, its controlled input being connected to power block 10 through a block of controlled constant voltage, made in the form of potentiometer 5.

Investigations of the signals of the proposed scheme for conformity to intermittent generation mode were conducted using digital oscillograph TDS 1012 with communication module with a computer of TDS 2CMA type [12]. The signals were registered in the drain of field transistor VT1 (Figure 1) at connection of single-coil ECP into the working circuit [11]. Standard specimen (SS) of SOP 5-1 type from aluminium alloy with an artificial defect of 2 mm length, 0.5 mm depth and 0.1 mm opening was used. Figure 2 shows signals, obtained when placing ECP at a distance from SS (in "air") (Figure 2, *a*) and in SS defect-free zone (Figure 2, *b*), with scanning time of 2.5 ms/div. ECFD was first set to maximum sensitivity to defects in the studied material. As we can see, the nature of the signal does not change, when ECP is placed in "air" and on SS surface. Here, when ECP is placed in "air", the period of repetition of series of high-frequency oscillations is 2 ms (frequency F = 500 Hz), and when ECP is installed on SS the period of repetition of series of high-frequency oscillations is reduced two times to 1 ms (frequency F = 1 kHz). Signal am-

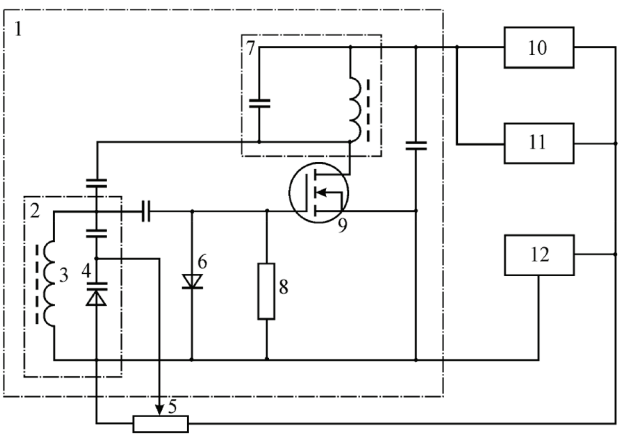

Figure 1. Circuit of self-generator ECFD based on field transistor with insulated-gate

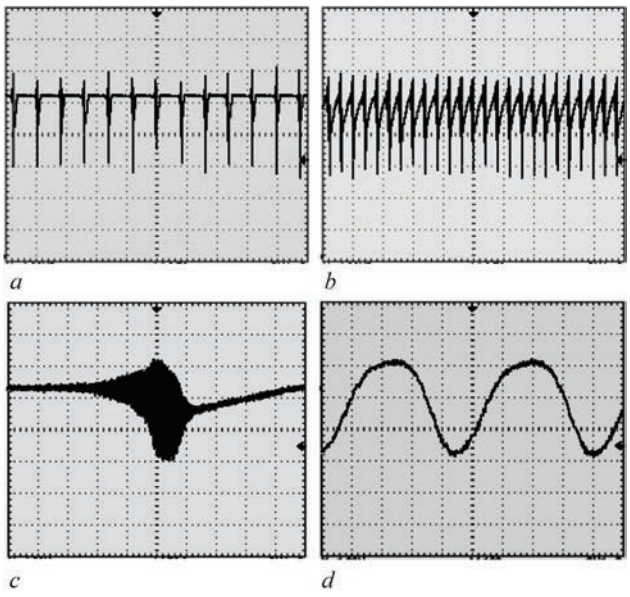

Figure 2. Signals in the drain of field transistor when ECP is placed in "air" (*a*) and in SS defect-free zone at scanning time of 2.5 ms/div (*b*), 50 μs/div (*c*), and 100 ns/div (*d*)

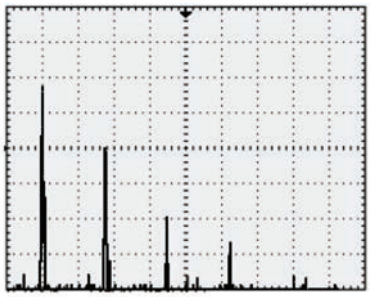

Figure 3. Signal spectrum in the drain of field transistor when ECP is placed in "air"

plitude when ECP is installed on SS is only slightly increased. Let us consider in greater detail the signal structure, when the oscillograph scan time in case of placing ECP in "air", was reduced from 2 ms/div (Figure 2, *a*) to 50 μs/div and 100 ns/div (Figure 2, *d*), i.e. the image was "stretched" on the time scale by 40 and 20000 times, respectively. High-frequency filling of the pulse of SG intermittent generation (Figure 2, *a*) can be seen in greater detail at reduction of scan time to 100 ns (Figure 2, *d*). The filling signals have a shape close to the sinusoidal one of 2.2 MHz frequency (Figure 2, *d*).

Figure 3 shows the spectrum of the signal, given above in Figure 2, which was obtained using digital oscillograph TDS 1012, which allows realization of the operation of fast Fourier transform [12]. The signal spectrum shows the components decreasing in amplitude, the distance between which is 2.2. MHz on the frequency axis, that corresponds to the frequency of high-frequency filling of the pulse in Figure 2, *d*.

Let us consider the dependencies of bias voltage U_b and frequency F of high-frequency oscillation series repetition on frequency f of SG high-frequency oscillations (Figure 2). Frequency f and frequency F of high-frequency oscillation series repetition were measured by digital oscillograph of TDS 1012 type by connection to the drain of transistor VT1 through 1:10 voltage divider. Bias voltage U_b was measured on the gate of transistor VT1 (Figure 1) by digital multimeter M890F with internal resistance of 20 MOhm/V, which was connected via 1 MOhm resistor to eliminate the influence of parasitic capacitance. Frequency f was changed by adjustment of SG working circuit. Investigations were conducted when positioning ECP in "air", as well as after installing ECP on SS from a nonferromagnetic alloy with SEC from 0.54 to 51.9 MS/m and on SS from ferromagnetic steel 45 for two control modes which correspond to highly conductive (aluminium alloys) and low conductive (titanium alloys, steels) materials. Generation suppression point (GSP in Figures 4, 5) was determined for each studied material and SG setting mode.

Analysis of the dependencies in Figures 4, 5 shows that suppression of SG oscillations for SS with different SEC for each mode of SG setting (and material group) is found at the same operational frequency f and bias voltage U_b. In modes of testing low conductive and highly conductive materials SG generates stable

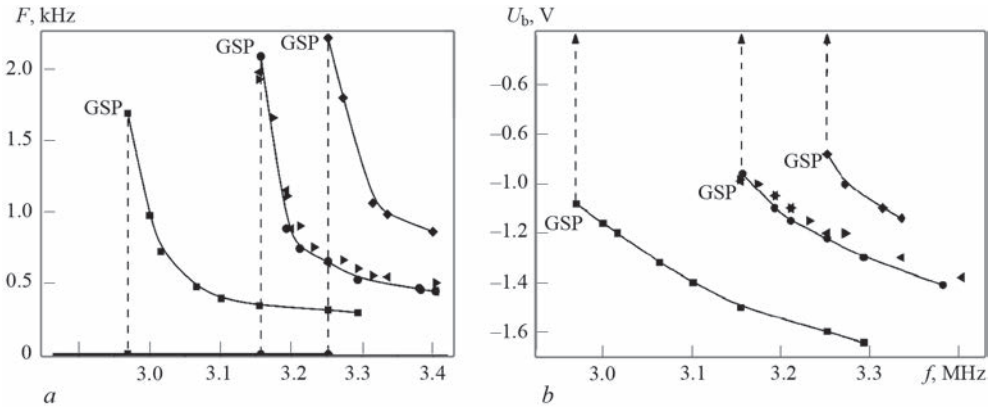

Figure 4. Dependence of frequency F of repetition of a series of high-frequency oscillations (*a*) and bias voltage U_b (*b*) of SG in the range of testing low-conductive materials on operational frequency f, when ECP is placed in "air" (■) and on SS with SEC of 0.54 MS/m (◄); 0.4 MS/m (►); 2.05 MS/m (●) and steel 45 (♦)

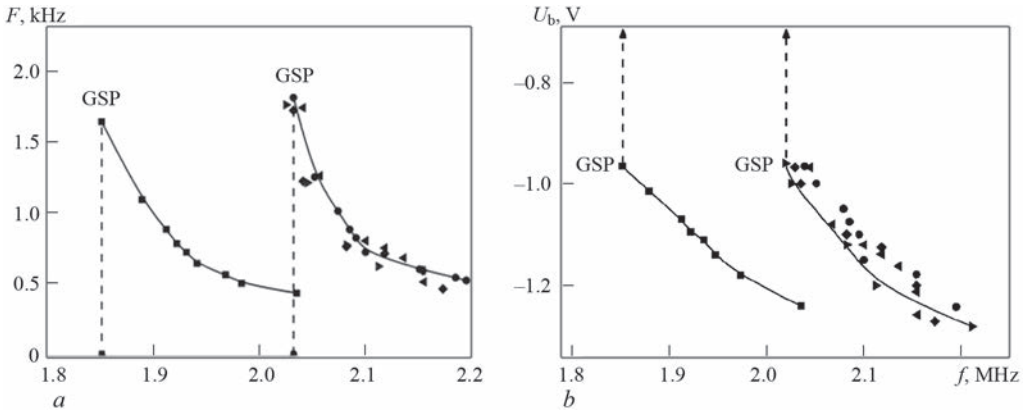

Figure 5. Dependence of frequency F of repetition of a series of high-frequency oscillations (*a*) and bias voltage U_b (*b*) of SG in the range of testing highly conducting materials on working frequency f when ECP is placed in "air" (■) and on SS with SEC of 11.0 MS/m (●); 14.8 MS/m (◄); 30.4 MS/m (►) and 51.8 MS/m (♦)

high-frequency oscillations in operational frequencies of 3.4 and 2.2 MHz that corresponds to the start of the studied frequency ranges. At reduction of frequency f (operational frequency) and respective increase of the difference in resonance frequencies of working and reference circuits Δf, the generation conditions deteriorate. It leads first to gradual increase of pulse repetition frequency F and generation suppression (GSP), which is shown in Figures 4, *a* and 5, *a* by a vertical dashed line. Steepness of the dependencies becomes greater, when moving closer to generation suppression point that confirms the high sensitivity of self-generator when setting it up into a mode close to this point (GSP in Figures 4, 5). At lowering of operational frequency f due to deterioration of generation conditions and reduction of high-frequency oscillation amplitude, bias voltage U_b decreases, until it reaches a certain value, at which generation suppression takes place. In the absence of high-frequency oscillations after oscillation suppression, bias voltage U_b decreases abruptly (vertical dashed line in Figures 4, *b* and 5, *b*) to zero.

Effectiveness of the developed SG circuit was studied experimentally by comparing the sensitivity of self-generator ECFD based on field transistors 2P303 (with closed *p-n*-transition) and 2P305 (with insulated gate). Change of the frequency of repetition of high-frequency oscillation series in intermittent generation mode at introduction of additional resistance of 47 kOhms into the working loop, was taken as the sensitivity criterion (Table 1). Before that, ECP was mounted on the defectfree part of SS from an aluminium alloy (SOP 5-1), titanium alloy (SOP 5-2) and ferromagnetic steel (SOP 5-3).

Presented results indicate that the sensitivity of the proposed ECFD circuit with SG based on a transistor with an insulated gate is higher for all structural materials. Sensitivity increases the most (by 1.5 times) for highly conductive nonferromagnetic materials and the least (by 1.2 times) — for a ferromagnetic alloy. Selection of an insulated-gate field transistor as an SG active element allows increasing the operating reliability of self-generator ECFD, when testing materials with different electrophysical properties and different gap between ECP and TO surface, owing to better technical characteristics of such a transistor, in particular, high input resistance, limit frequency and transient slope.

2. IMPROVEMENT AND INVESTIGATION OF SELF-GENERATOR FREQUENCY CONTROL CIRCUIT

To set ECFD to the mode of maximum sensitivity, when testing materials with different electrophysical properties, the resonance frequency of SG working loop should be readjusted, for which purpose variable capacitance capacitors are used. In outdated self-generator ECFD adjustment of frequency is performed using variable capacitors with air or solid dielectric, which have a significant drawback of large overall dimensions and low reliability. More promising is the electronic method of readjustment, using semiconductor diodes (varicaps), the capacitance of which depends on reverse (cut-off) voltage applied to the *p-n*-junction. Small dimensions of varicaps allow placing them near SG active element. The length of contact leads to control the varicap capacitance is not

Table 1. Comparison of sensitivity of ECFD with SG based on transistors of different types

Transistor type	ECP on SOP-5-1			ECP on SOP 5-2			ECP on SOP 5-3		
	F_1	F_2	ΔF	F_1	F_2	ΔF	F_1	F_2	ΔF
2P 303	2.38	2.22	0.16	3.23	2.71	0.52	3.23	2.63	0.60
2P 305	1.59	1.35	0.24	2.33	1.70	0.63	2.50	1.72	0.78

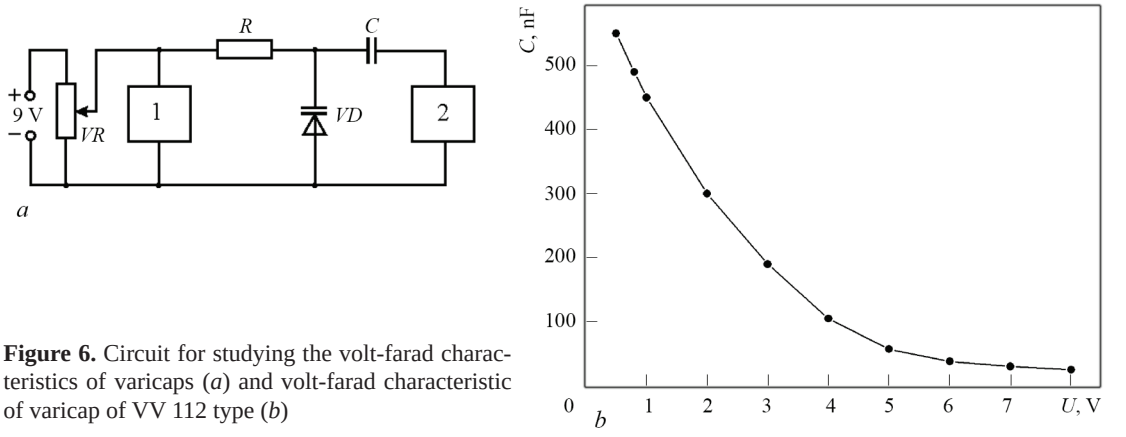

Figure 6. Circuit for studying the volt-farad characteristics of varicaps (*a*) and volt-farad characteristic of varicap of VV 112 type (*b*)

a critical value, as control is performed using constant voltage. Smoothness of adjustment using a potentiometer is better than that of a replaceable capacitor. For instance, a replaceable resistor of SP3-33 type allows rotating the axis by an up to 320° angle, that is 1.8 times greater than the angle of rotation of a replaceable capacitor. Varicaps have been known for a longtime, but the industry has only recently mastered production of varicaps with a high *Q*-factor (*Q*×200) with readjustment range by capacitance from 30 up to 600 pF and small dimensions (3.8×1.6 mm). Comparative analysis showed that the most promising for construction of self-generator ECFD is varicap of VV 112 type, which in addition to a high *Q*-factor has the best overlap ratio and temperature stability. VV 112 varicap is controlled by voltage from 0.5 up to 8.0 V that makes it applicable for instruments with autonomous power supply. It is important that VV 112 varicap has the lowest reverse current I_r, which is a constant parasitic current that flows through the varicap in the reverse direction at the set reverse voltage.

The main disadvantage of the varicaps is a low *Q*-factor, which even in the best varicaps is by an order of magnitude lower than that of ceramic capacitors, and by two-three orders lower than that of air capacitors. We will assess the possible influence of varicap of VV 112 type with $Q_v = 200$ on the *Q*-factor of oscillatory system as a whole. For this purpos we will use the expression for equivalent factor Q_E of an oscillatory system from connected in parallel capacitor and inductance of ECP winding with Q_{ECP} factor [13], which has the form of $Q_E = Q_{ECP}Q_v/Q_{ECP} + Q_v$. For the used basic ECP, Q_{ECP} winding factor has the value from 11.0 to 24.0, depending on TO material. It is obvious that in this case the *Q*-factor of SG oscillatory system will be limited predominantly by *Q*-factor of ECP winding. Connection of varicap of VV 112 type lowers the *Q*-factor of SG oscillatory system by 10–12 %, which can be regarded as insignificant, considering other advantages, the more so since the conducted assessment characterizes the worst case, when varicap *Q*-factor is the smallest at minimum value of control voltage $U_{min} = 0.5$ V.

The varicap operating mode should take into account its volt-farad characteristic, which was studied for varicap VV 112 using voltmeter of M 890 F type and CLR 2 meter of E 7-13 type (Figure 6, *a*). Varicap VD is connected to potentiometer VR 1 through resistor $R = 100$ kOhm, the role of which consists in protection of varicap VD and meter CLR 2 of E 7-13 type at the lower position of mobile electrode of VR potentiometer. Voltage on resistor *R* must be much lower than the smallest value of control voltage $U_{min} = 0.5$ V. Voltage across resistor *R* is determined by varicap reverse current ($I_r = 5 \cdot 10^{-8}$ A) and it is equal to $R \cdot I_r = 5$ mV, i.e. $R \cdot I_r << U_{min}$, that allows ignoring the influence of resistor *R* on measurement error. Capacitor *C* was introduced for protection of CLR meter of E 7-13 type from constant voltage penetration. Here, capacitance $C = 0.1$ μF, i.e. it is selected to be much higher than the varicap maximum capacitance ($C_{max} = 620$ pF) that allows ignoring its influence.

Volt-farad characteristics of VV 112 varicap (Figure 6, *b*) is nonlinear. Minimum and maximum values of control voltage are $U_{min} = 0.5$ V and $U_{max} = 8$ V, respectively. One can see from Figure 6, *b* that the change of control voltage from 6 to 8 V has little effect on varicap capacitance. Therefore, it is rational to limit the maximum value of control voltage by 6 V, at which minimum value of varicap capacitance C_{min} is equal to 50 pF.

The effectiveness of electron control of SG frequency depends on the scheme of varicap connection into the oscillatory circuit. Traditional varicap connection to control SG frequency is given in Figure 7, *a* [13, 14]. With the traditional circuit of varicap VD connection at low control voltage, it begins conducting current during the negative half-wave of SG high-frequency oscillations that leads to their distortion. Moreover, the oscillatory circuit receives additional load, leading to lowering of its *Q*-factor and sensitivity to changes of ECP parameters. Influence of this

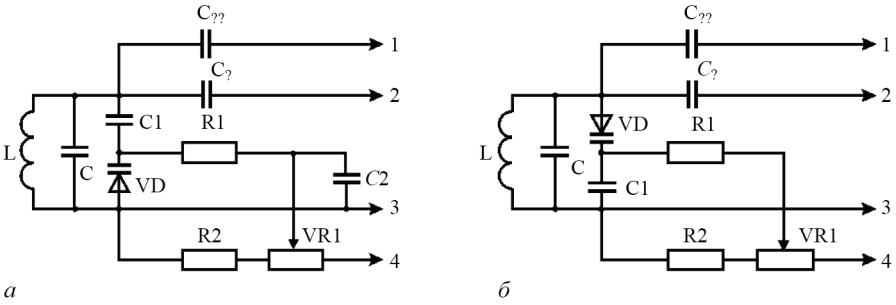

Figure 7. Traditional (*a*) and proposed (*b*) schemes for connection of VD varicap into SG working circuit: 1–4 — leads of SG feedback, control electrode of SG active element, common wire and supply voltage, respectively

factor was reduced in the proposed scheme of varicap connection into SG working circuit (Uchanin V.M., Cherlenevskyi V.V. Device for eddy current testing. Patent of Ukraine: 42132, 2009, Bul. No. 12). In the proposed circuit (Figure 7, *b*) at low control voltage varicap current will influence the positive half wave of high-frequency oscillations. It, however, affects the operation of automatic bias circuit, which maintains a constant level of oscillation amplitude. Moreover, in the proposed circuit the influence of noises introduced into SG working loop by mobile contacts of variable resistor VR, which may reach 15–50 mV, is reduced due to filtration by R1 and C1 elements. It allows reaching a more accurate SG setting to a mode close to generation suppression, and making full use of the high sensitivity of the circuit.

Let us consider the influence of varicap capacitance on amplitude-frequency characteristics (AFCh) of oscillatory system of self-generator ECFD (Figure 1). Here, SG was brought into the mode of high-frequency regenerative amplifier. For this purpose, generation was suppressed by reducing the active element supply voltage. ECP was connected to flaw detector SG by a coaxial cable, which is part of the oscillatory system [15]. To eliminate shunting of the working circuit by low output resistance of the generator, the outer generator signal was introduced through coupling capacitor of 10 pF capacitance, as it has to be much smaller than the minimum value of working circuit capacitance. Minimum value of working loop capacitance is equal to 150 pF, as in keeping with the above assessments, it consists of cable capacitance (100 pF) and smallest value of varicap capacitance (C_{min} = 50 pF). To eliminate the influence of elements of automatic bias circuit on oscillatory system AFCh, the voltage amplitude of external generator was selected equal to 1 V. Here, voltage amplitude in the working loop is not higher than 15 mV, i.e. it is much smaller than the voltage of 200 mV, from which diode 6 (Figure 1) of SG automatic bias circuit starts operating. Millivoltmeter was connected to drain loop of transistor 9 (Figure 1) by a high-frequency head. Investigations were conducted, placing ECP in "air" at the highest values of varicap capacitance and in the defect-free part of SS of SOP 5-1 type (D16 aluminium alloy) at the highest and lowest values of varicap capacitance.

Each of the obtained AFCh (Figure 8) has two resonance maximums which is characteristic for SG double-circuit oscillatory system. Here, the maximum amplitude of the reference loop is greater than that of the working circuit in the entire range of varicap capacitance change that is attributable to higher *Q*-factor of the reference loop, compared to that of the working circuit ($Q_{ref} \approx 90$, $Q_{work} \approx 20$). When ECP is installed on SS the amplitude decreases in both the maximum points for all the modes that is attributable to lowering of ECP winding *Q*-factor at interaction with SS from an aluminium alloy. At the change of varicap capacitance from the minimum (C_{min} = 50 pF) to maximum one (C_{max} = 620 pF), the value of working circuit resonance frequency is increased by 1.3 MHz, and the loop resonance frequencies become closer. At the same time, the amplitude in the point of maximum of the working circuit characteristic is increased. Here, the resonance frequency of the reference circuit does not change noticeably, that is also attributable to higher *Q*-factor of the reference circuit.

The presented procedure of determination of oscillatory system AFCh was used for ECFD adjustment during their manufacture, as it allows revealing the el-

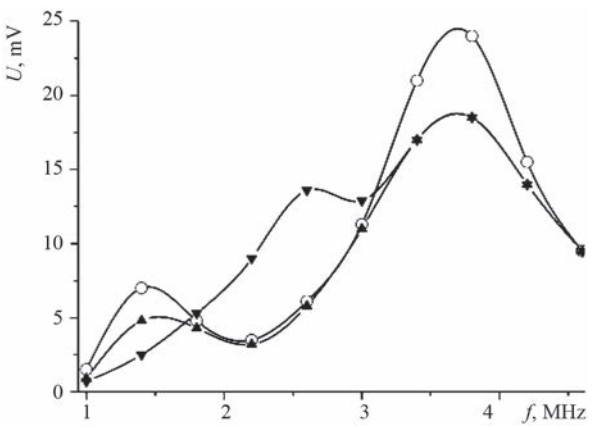

Figure 8. Amplitude-frequency characteristics of oscillatory system of SG: when ECP is in "air" at the highest value of varicap capacitance (○) and on defectfree part of SS from aluminium alloy at the highest (▼) and lowest (▲) values of varicap capacitance

Table 2. Comparison of SG sensitivity with different varicap connections

Circuit	ECP on SOP 5-1			ECP on SOP 5-2			ECP on SOP 5-3		
	F_1	F_2	ΔF	F_1	F_2	ΔF	F_1	F_2	ΔF
Traditional (Figure 7, *a*)	1.59	1.35	0.24	2.33	1.70	0.63	2.50	1.72	0.78
Proposed (Figure 7, *b*)	1.61	1.28	0.33	2.13	1.22	0.91	2.33	1.28	1.05

ements with a low *Q*-factor (for instance, poor quality capacitors) and ensure ECP replaceability due to improvement of repeatability of ECFD characteristics.

Comparison of the sensitivity of self-generator ECFD with application of the traditional and new SFCC was conducted by the above procedure, where the sensitivity criterion was taken to be the change $\Delta F = F_1 - F_2$ of the frequency of repetition of a series of high-frequency oscillations, at introduction of additional resistance of 47 kOhm into the working loop, when ECP is mounted on defect-free zone of SS from an aluminium alloy (SOP 5-1), titanium alloy (SOP 5-2) and ferromagnetic steel (SOP 5-3). All studied ECP were based on a field transistor with an insulated gate. Measurement results are given in Table 2.

Results presented in Table 2 show that the sensitivity of ECP with the proposed SFCC is higher than that of the traditional circuit by 1.38; 1.44 ad 1.35 times for aluminium and titanium alloys and ferromagnetic steels, respectively, i.e. it allows achieving a higher sensitivity during testing all structural materials.

3. SORC IMPROVEMENT AND INVESTIGATION

The main function of SORC is fast resumption of SG oscillations after detection of the defect, and respective generation suppression. It is achieved by improvement of oscillation generation conditions by increasing the supply voltage. In the first self-generator ECFD such circuits were absent and regeneration was performed by removing ECP from TO surface [1]. ECP lifting from TO surface improves its *Q*-factor and reduces the losses in the oscillatory loop. It is obvious that such a procedure of resumption of SG oscillations complicates the procedure and productivity of testing. Later on relaxation generators were used for oscillation regeneration. They were connected into the supply circuit of SG active element and were started after suppression of its generation. Periodical increase of supply voltage of self-generator active element leads to improvement of generation resumption conditions. Self-generator ECFD of TVD type, in particular, includes SORC, in which the relaxation generator consists of a current-stabilizing element, delay line based on single-junction transistor with RC-circuit, which sets the frequency of relaxation oscillations, and a key, switching of which leads to a periodical increase of supply voltage [4].

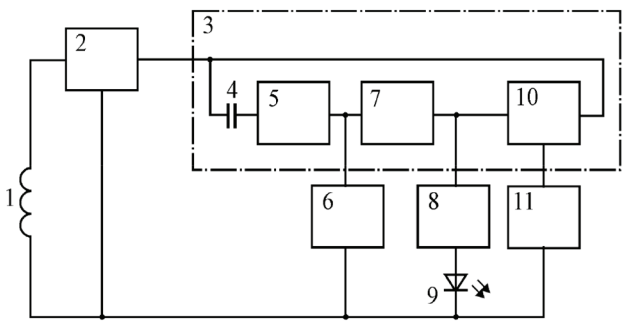

Figure 9. Block-diagram of ECFD with improved SORC

Analysis of the conditions, promoting resumption of SG oscillations, allowed suggesting a new SORC (Uchanin V.M., Cherlenevskyi V.V. Eddy current self-generator flaw detector. Patent of Ukraine, Pat. 39217, 2009, Bul. No. 3), which, owing to its fast response, allows greatly improving the testing productivity, compared to analogs, and which, in principle, can operate with SG based on different active elements. Let us consider the operation of an improved SORC (Figures 9–11). When ECP 1 is mounted on a defectfree region of TO, self-generator 2 generates intermittent oscillations near the generation suppression point (GSP in Figures 4, 5), which are heard as changed-tonal sound of sound indicator 6. When a defect arises, the *Q*-factor of ECP 1 decreases, leading to reduction of *Q*-factor of the working circuit of SG 2 and oscillation suppression. SG 2 output signal via capacitor 4 comes to limiting amplifier 5, which forms a signal of sound frequency. This signal come to sound indicator 6 and to the input of defect signal former 7, which forms a short pulse at its appearance, the amplitude of which changes from supply voltage value to zero. A short pulse comes to transistor regulator of current T2 via diode D4 of supply voltage control circuit (Figure 11). Current regulator transistor T2 opens, leading to increase of SG 2 supply voltage. As a result, intermittent oscillations of SG 2 are resumed provided ECP 1 is shifted from the defect, and SG 2 is ready for further operation. When ECP is located on the defect, the process of lowering and subsequent increase of SG 2 power supply is repeated with the frequency close to 100 Hz. The repetition frequency of these pulses is in the sound range and after amplification it is recorded by sound indicator 6. A short pulse from the output of defect signal former 7 comes

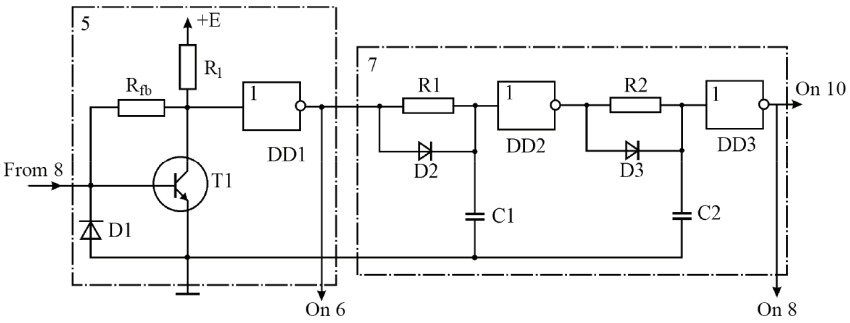

Figure 10. Circuit of limiting amplifier and defect signal former of SORC: D1 — diode; R_{fb} — feedback resistor; R1, R2, C1, C2, D2 and D3 — integrating diode circuits; DD1, DD2, DD3 — inverters

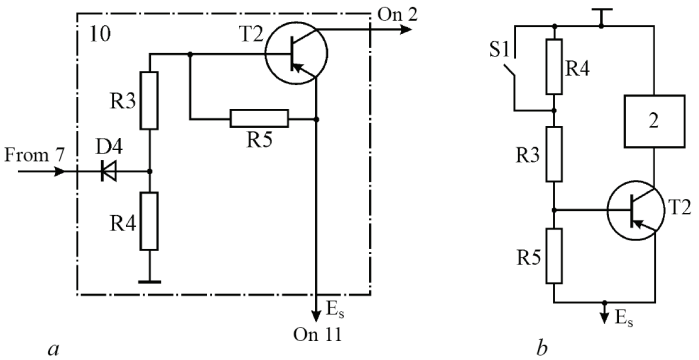

Figure 11. Circuit of supply voltage control (*a*) and its equivalent circuit (*b*): D4 — switching diode; R3 and R5 — supports of base voltage divider; T2 — transistor current regulator; 2 — SG; S1 — switch

to pulse expander 8, which increase the pulse length until defect light indicator 9 lights up.

Operation of SORC elements was studied, recording the signals in different SORC elements with digital oscillograph of TDS 1012 type, fitted with expansion module TDS 2CMA (see Figures 12, 13). Division value along the vertical is 1 V, along the horizontal it is 2.5 ms. In addition, the parameters of individual SORC elements are calculated below.

Limiting amplifier 5 (Figures 9, 10) is based on transistor T1, which is connected into a circuit with a common emitter with negative voltage feedback through feedback resistor R_{fb}. Isolation capacitor 4 (Figure 9) passes only the variable component of SG output voltage to the base of transistor T1. Diode D1 eliminates negative halfwave of input signal and binds it to logic zero level. Figure 12, *a*, *b* shows signals at SG output (before capacitor 4), and Figure 12, *c*, *d* — signals at the base of transistor T1 of limiting amplifier 5 in the absence of a defect and at ECP location on the defect, respectively. When ECP is located outside the defect (Figure 12, *a*), stable oscillations of 1 kHz frequency and amplitude close to 1 V are observed at SG output together with the constant component of supply voltage of 6 V. When the converter is positioned on the defect (Figure 12, *b*), suppression of oscillations is observed. Oscillatory process fades away because of the low *Q*-factor of ECP working loop when it is located on the defect, and supply voltage decreases to the ground level, due to increase in SG current consumption. It leads to repeated suppression of generation, which is indicated by signal skip areas in Figure 12, *b*, *d*. While ECP is on the defect, this process is repeated with a frequency close to 100 Hz. A variable useful signal without the constant component remains after the capacitor (Figure 12, *c*, *d*), which carries information about ECP position on the surface of TE or about the defect. Transistor T1 of *n-p-n* type operates in the key mode and it is controlled by a signal of positive polarity: in the absence of the signal the transistor is closed, current is absent and supply voltage of 6 V is set on the collector. Amplified signal at the collector of transistor T1 (Figure 12, *e*, *f*) is limited from below by ground potential level, and from above — by the supply voltage. Time lapses in Figure 12, *f*, in which there is no signal, are indicative of ECP being on the defect. Transistor T1 should amplify the minimum value of SG output signal to the level of supply voltage E_s, i.e. ensure the level of logical unit with an excess. Minimum output voltage U_{min} is equal to approximately 0.2 V, and the supply voltage level is 6 V. Hence, the gain of limiting amplifier should correspond to the condition of $K \geq E_s/U_{min} = 30$. For the selected maximum collector current of the transistor $I_c = 0.4$ mA, the load resistance will be $R_l = E_s/I_c = 15$ kOhm. As amplification coefficient is equal to ratio $K = R_{fb}/R_l$, then to ensure the required amplification, feedback resistance R_{fb} was selected greater

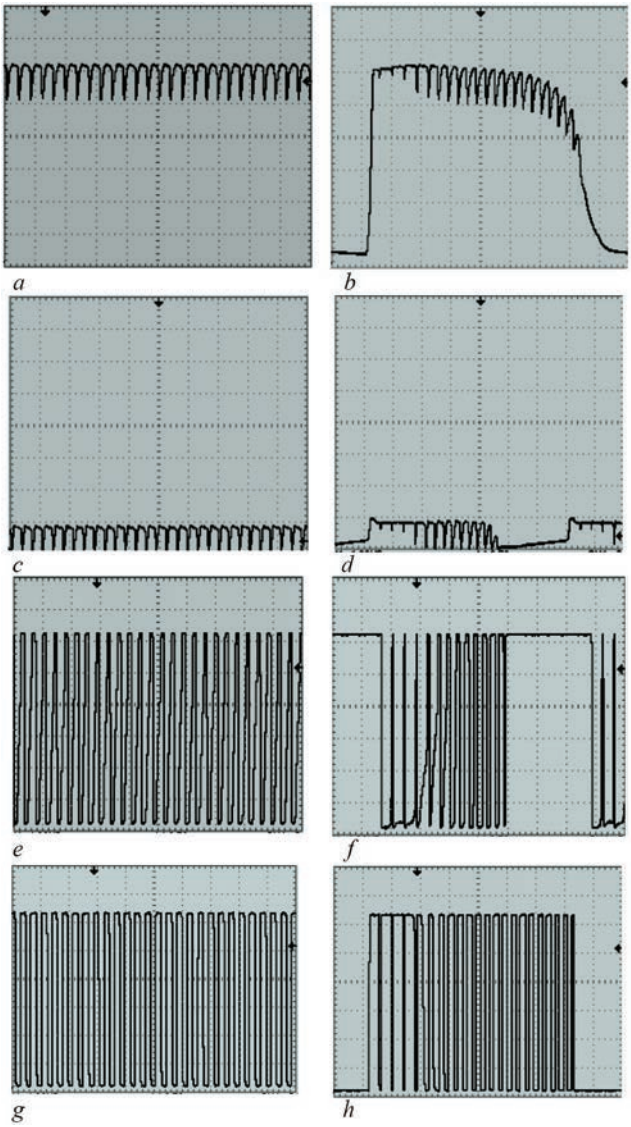

Figure 12. SORC signals in the absence of defect (left) and when ECP is placed on the defect (right): *a*, *b* — at SORC input; *c*, *d* — at T1 transistor base; *e*, *f* — at inverter input; *g*, *h* — at DD1 inverter output (Figure 10)

than 450 kOhm. Output signal of logic inverter DD1 forms change-tonal information about the defect and ECP position on TO surface, and comes to sound indication block 6, which consists of low-frequency amplifier and operator headphones. DD1 logic inverter performs signal inversion and additionally amplifies them to the level of supply voltage to improve the rectangular shape of the signal (Figure 12, *g*, *h*). DD1 logic inverter was built using MC 14069 UDP microcircuit of Motorola Company, which has 6 separate inverters, which are also used for other SORC elements. Circuit parameters are as follows: logic zero output level ≤ 1 % E_s, logic unit output level — 9.95 % E_s, logic zero input level ≤ 20 % E_s, logic unit input level ≥ 80 % E_s. Supply voltage E_s can be selected in the range of 3–18 V.

Sound frequency signal from DD1 inverter output comes to signal former, which, in order to sharpen the defect signal pulse, is made in the form of two integrating circuits R1–C1–D2 and R2–C2–D3, connected in series, with DD2 and DD3 inverters (Figure 10). The time constant $\tau = R \cdot C$ of integrating circuits is selected to be such as to smooth the signal of sound frequency of 1–3 kHz, which corresponds to TO defectfree region. The integrating circuit plays the role of a filter to suppress the signal. Therefore, we define the attenuation factor as equal to $k_{att} = U_{in}/U_{out} \geq \geq 100$. Hence, the parameters of equivalent scheme of integrating circuit are defined by the following relationship ($R + X_c/X_c \geq 100$ or $R \geq 99X_c$, where R and X_c are the resistance and reactance of the resistor and capacitor of integrating circuits (Figure 10). Capacitor capacitance was selected equal to 47 nF. Then, reactance X_c = 3390 Ohm for the lowest signal frequency (1 kHz) to be suppressed. Hence, resistor resistance R should be selected greater than X_c = 3390 Ohm.

In Figure 12, *a* the remains of the sound signal of approximately 1 kHz frequency are observed on the level of logic unit, which disappear after the next integrating circuits (Figure 13, *c*, *e*, *g*), and the signal in the defectfree area is smoothed. Here, the integrating circuits pass the low-frequency signal with repetition rate of pulse series close to 100 Hz, which correspond to periodical suppression of SG oscillations at ECP positioned on the defect. DD2 and DD3 inverters are used to form a short pulse (Figure 13, *h*) with steep fronts for starting the supply voltage control circuit, which also comes to pulse expander 8 (Figure 9) to form the pulse, designed for light diode operation. In Figure 13, *b* the start of formation of the pulsed signal from the defect is observed in the absence of intermittent generation, when ECP is located on the defect. Signal amplitude in $t_2 - t_3$ time range decreases by the following exponential law $U(t) = E_s e^{-t/\tau}$, where $U(t)$ is the voltage at moment of time t. Steep fronts of pulsed signal from the defect are reached by adding D2 diode, through which fast charging of C1 capacitor takes place at moment of time t_1. C1 capacitor discharges slowly through R1 resistor. Further forming of defect signal occurs similarly in the other R2C2 integrating circuit and DD3 inverter. In TO defectfree area a line is observed at logic zero level at the output of integrating circuit R2C2 (Figure 13, *e*). On the defect (Figure 13, *f*) the signal at the output of R2C2 integrating circuit increases abruptly due to C2 capacitor charging through D2 diode and decreases slowly by exponential law through its discharging to R2 resistor. A short negative pulse with steep fronts of approximately 2.5 ms duration signaling about the defect, forms at the output of DD3 inverter (Figure 13, *h*). In the absence of the defect, the signal at the output of DD3 logic inverter has only a constant component

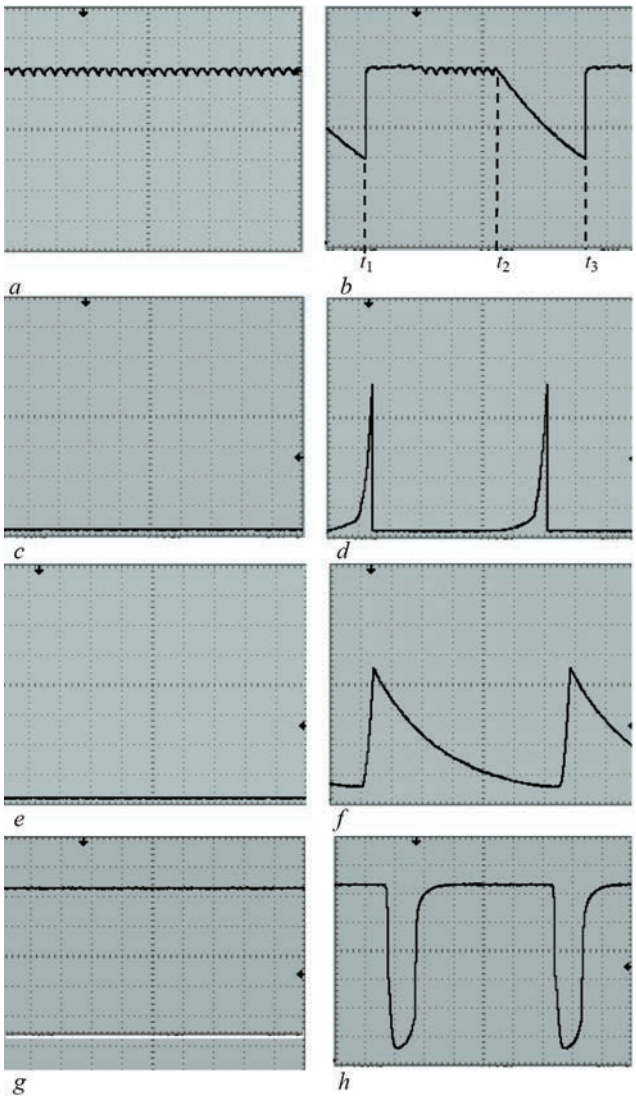

Figure 13. SORC signals in the absence of defects (left) and when ECP is placed on the defect (right): *a*, *b* — at DD2 inverter input; *c*, *d* — at DD2 inverter output; *e*, *f* — at DD3 inverter input; *g*, *h* — DD3 inverter output

at the level of logic unit (Figure 13, *g*). The signal from the defect (Figure 13, *h*) comes to SG supply voltage control circuit, which is a controlled current source based on T2 transistor of *p-n-p* type, connected in a circuit with a common emitter (Figure 13, *a*). In the equivalent circuit (Figure 13, *b*) electronic switch based on D4 diode is replaced by S1 switch. Supply voltage E_s is divided into collector-emitter voltage U_{ce} of T2 transistor and SG voltage U_{SG} $E_s = U_{SG} + U_{ce.}$ R3, R4 and R5 supports are part of base voltage of T2 transistor and determine its current according to $I = E_s/(R_3 + R_4 + R_5)$ ratio. In its turn, the change of base current influences the collector current of T2 transistor, which passes through SG 2 active element. At generation suppression on the defect, a pulse forms at the output of former 7 (DD3 inverter). This pulse shorts the cathode of D4 diode to the ground for 2.5 ms, and reduces the influence of R4 resistor due to shunting. In the equivalent circuit it is modeled by shorting S1 switch to the ground. Here, base-emitter voltage U_{be} of T2 transistor increases, reducing the equivalent resistance of T2 transistor and its U_{ce} voltage. The voltage in SG active element increases due to redistribution of stabilized voltage, leading to resumption of its generation.

The advantage of the proposed SORC consists in that, in addition to fast resumption of SG oscillations after their suppression, it also ensures convenient connection of the sound and light indicators and use of integral CMOS of logic inverters with low current consumption ($1.5 \cdot 10^{-6}$ A) and low supply voltage.

CONCLUSIONS

SG scheme circuit with double-circuit oscillatory system, operating in intermittent generation mode, is promising for development of self-generator ECFD. New engineering solutions were proposed and studied, in particular SG circuit based on a field transistor with an insulated gate, circuit of generation frequency control and circuit of SG oscillation regeneration. Their advantages concerned with sensitivity are shown, compared to traditional schemes. The analyzed engineering solutions were used to develop self-generator ECFD of VD 3.03N, VD 3.02N, VD 4.01N and VD 4.03N type to reveal surface cracks, which have passed state testing, and have been entered into the State Register of measuring equipment. They are used for maintenance of aircraft of SC "Antonov" and aircraft engines of SC "Ivchenko-Progress", as well as PJSC "Motor-Sich". The instruments have also been implemented in "International Airlines of Ukraine" Company, in Lviv and Konotop Aircraft Repair Enterprises, HPU "Lvivhasvydobyvannya", SPC "Zond", PJSC "Zakhidenergo", Karpaty and Poltava ETC, etc.

Practical experience of NDT using the developed ECFD confirmed the effectiveness of engineering solutions, presented in this paper. It is envisaged to apply them in the new intellectual self-generator ECFD, which will additionally have automatic adjustment to the sensitivity level, assigned by the testing procedure and indication of sensitivity level.

The paper is devoted to the bright memory of Vsevolod Vadymovych Cherlenevskyi, talented engineer, who directly participated in finding some of the engineering solutions and performing part of the measurements.

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